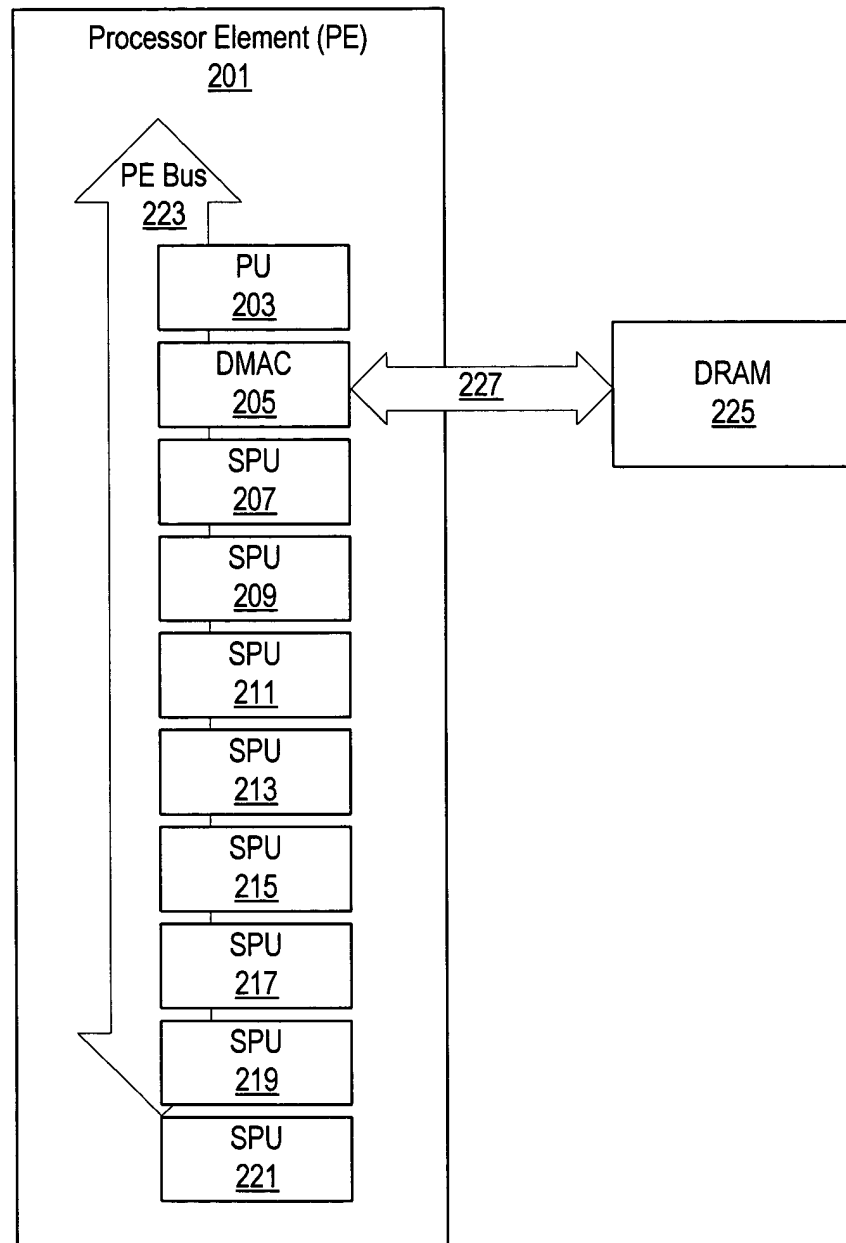
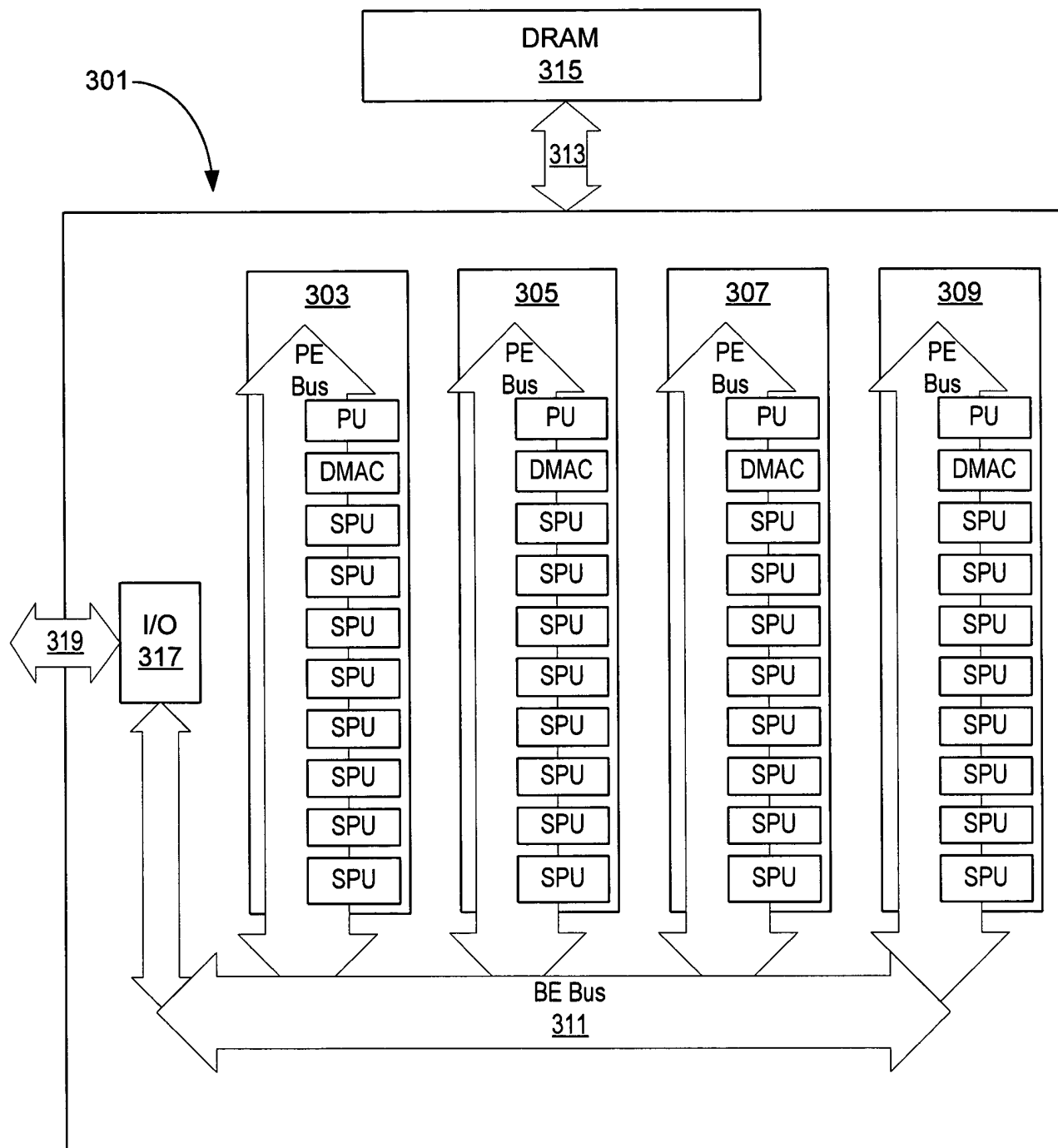
**Figure 1**

**Figure 2**

**Figure 3**

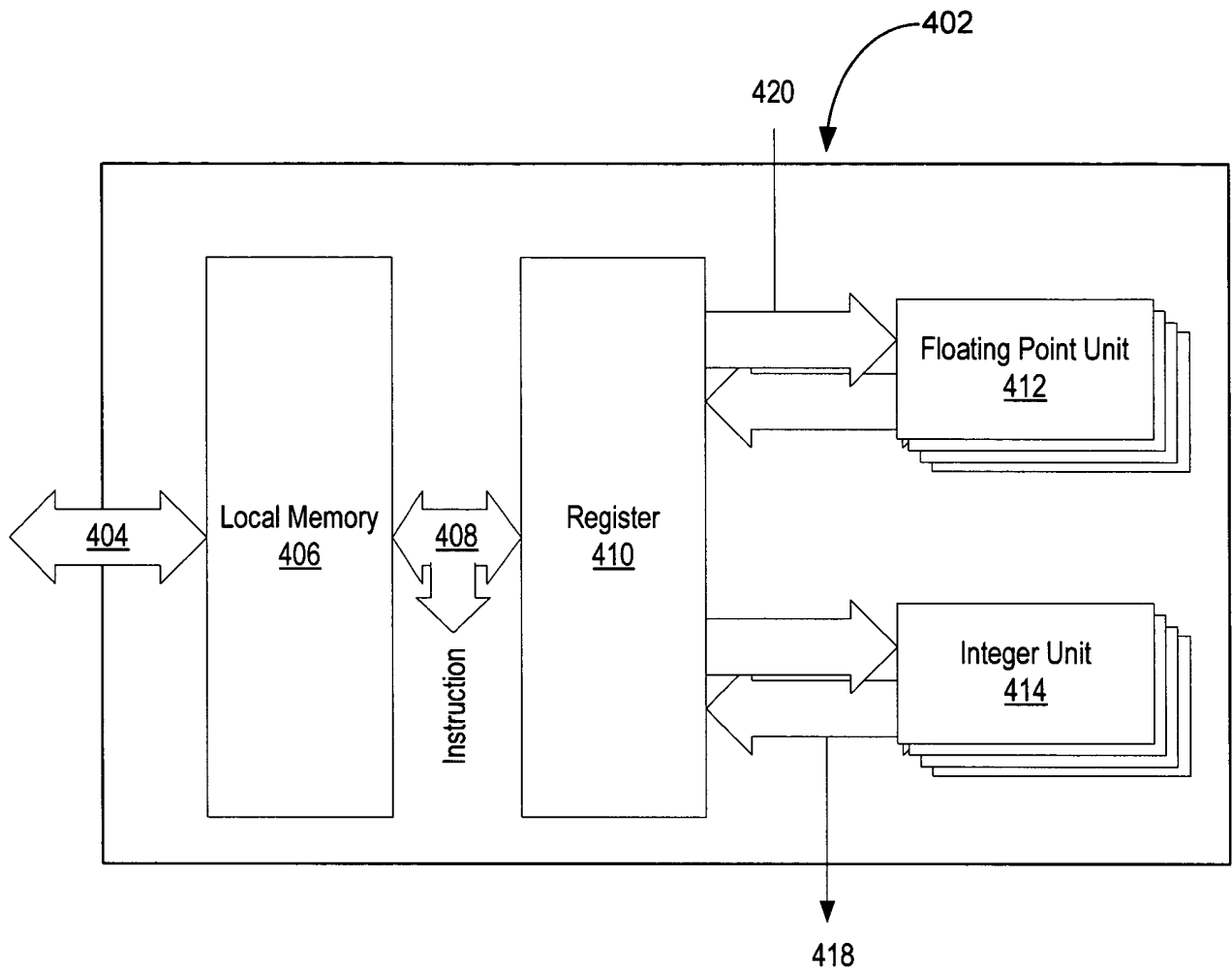


Figure 4

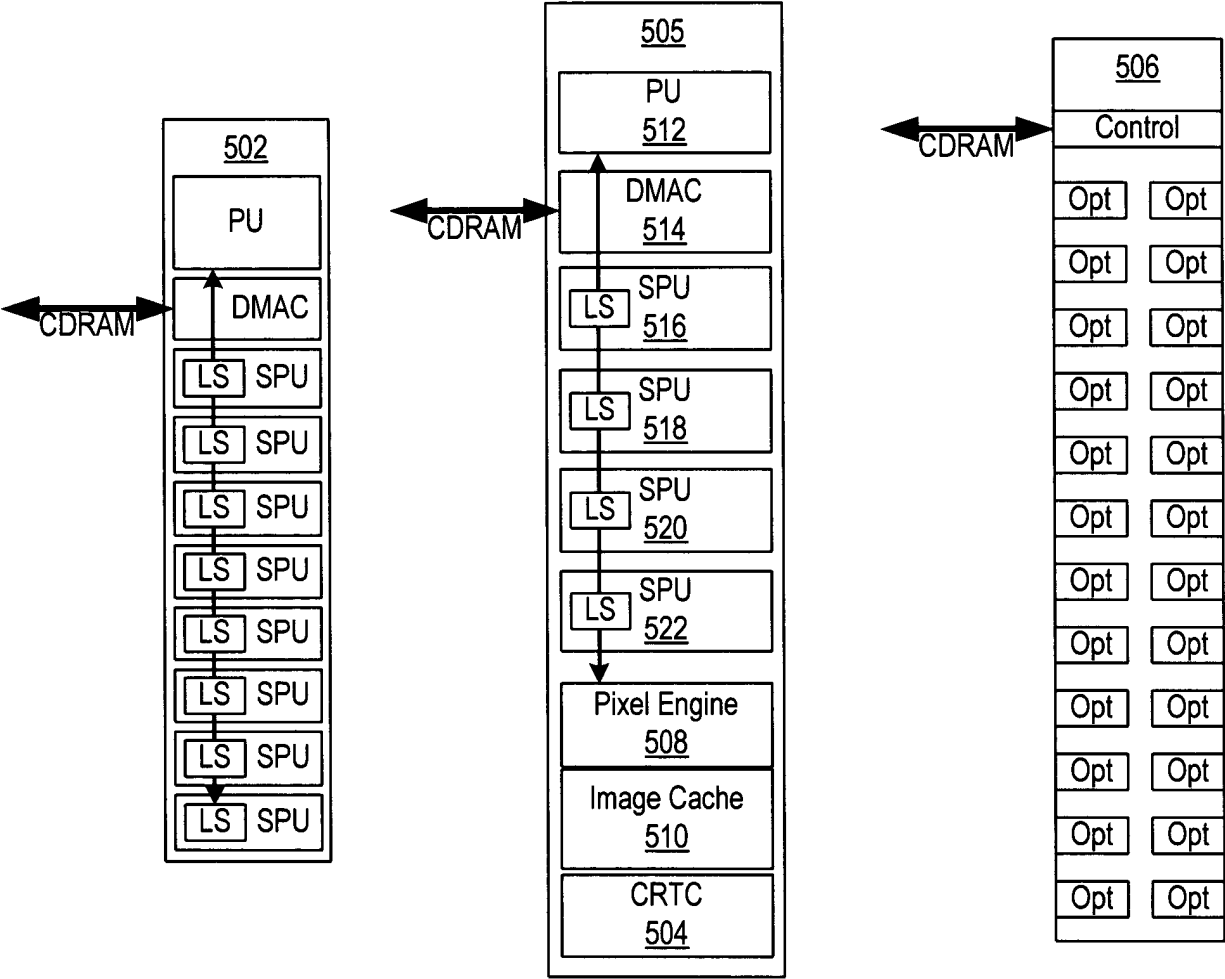


Figure 5

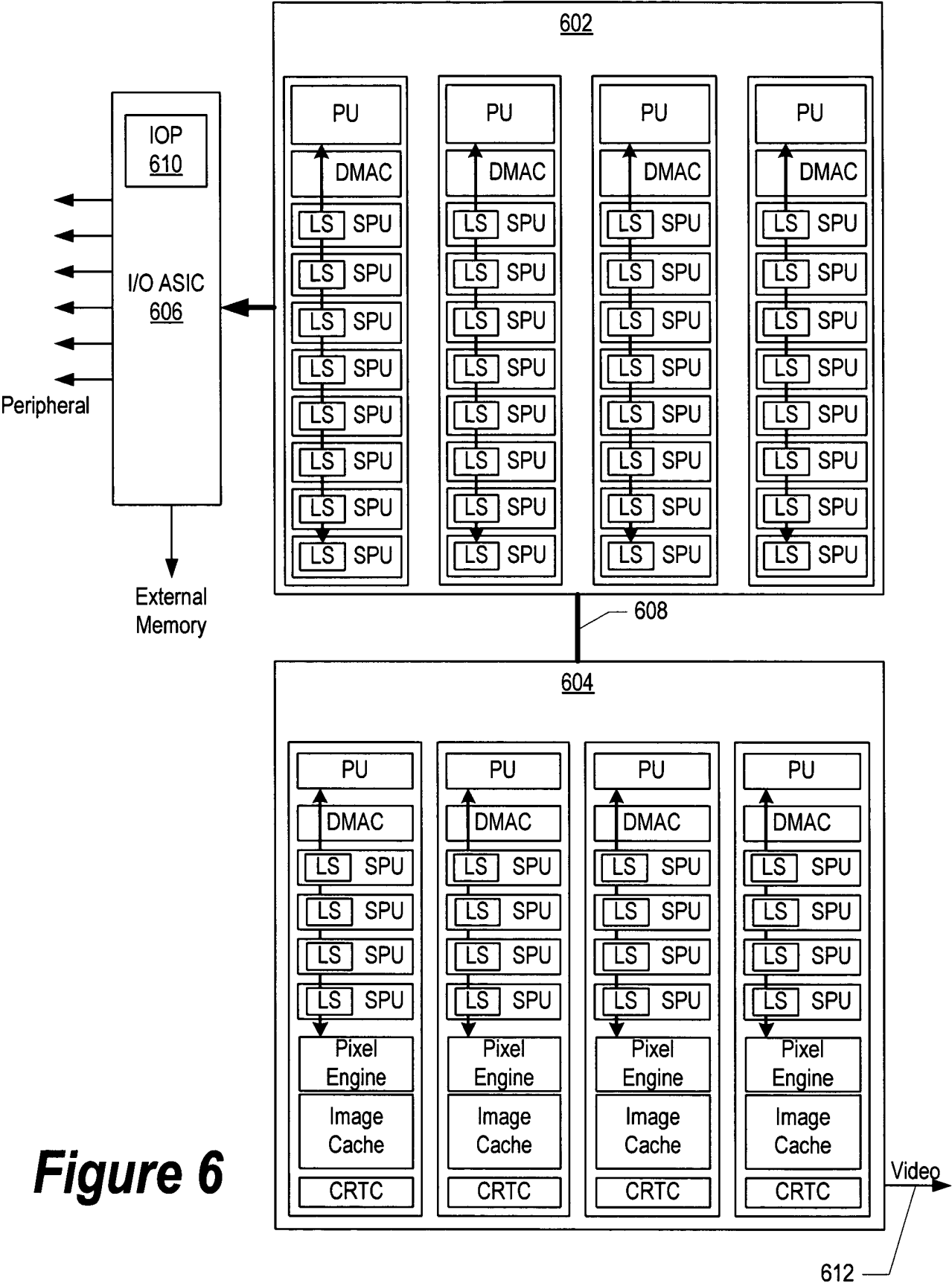
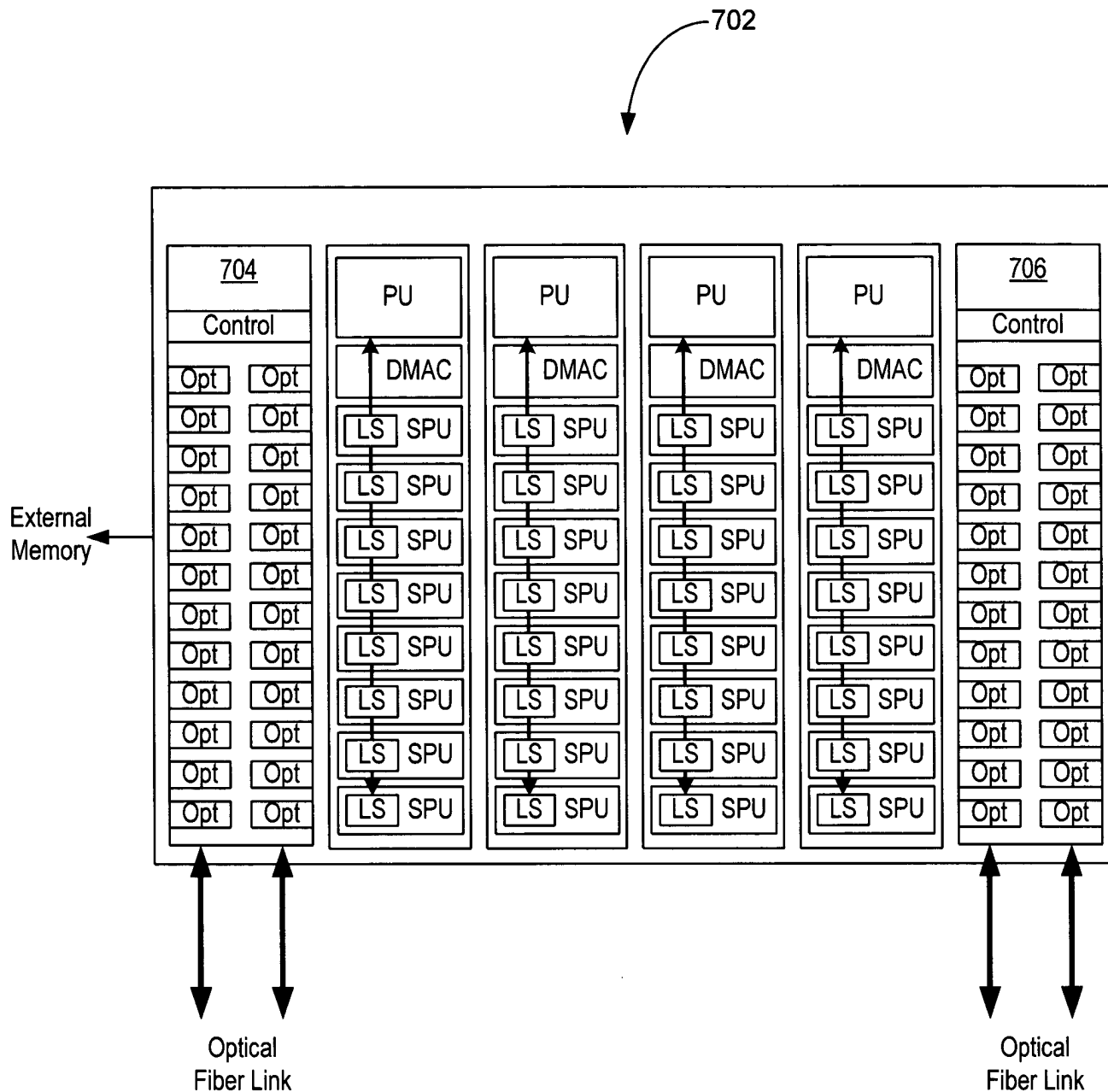


Figure 6

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**Figure 7**

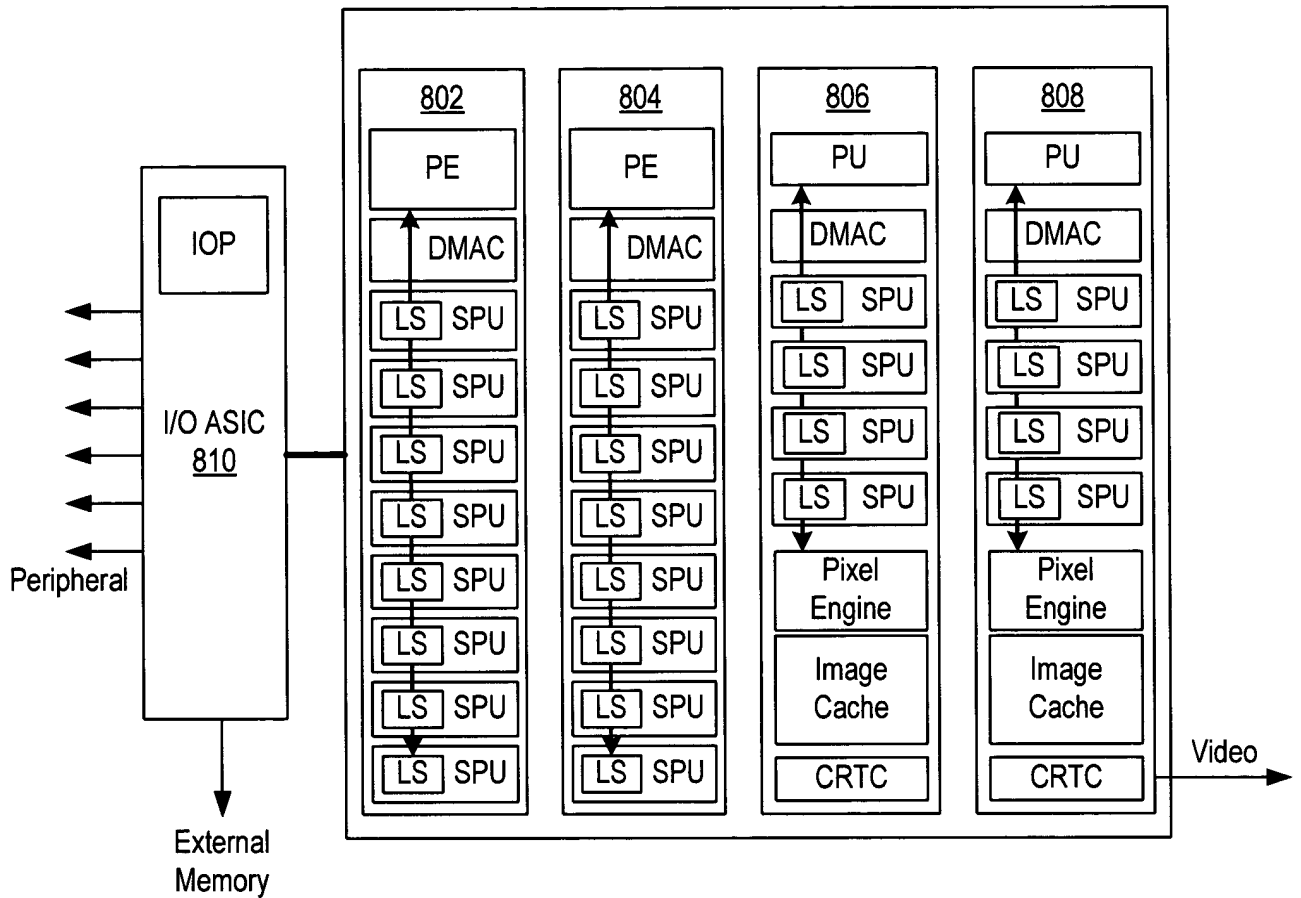
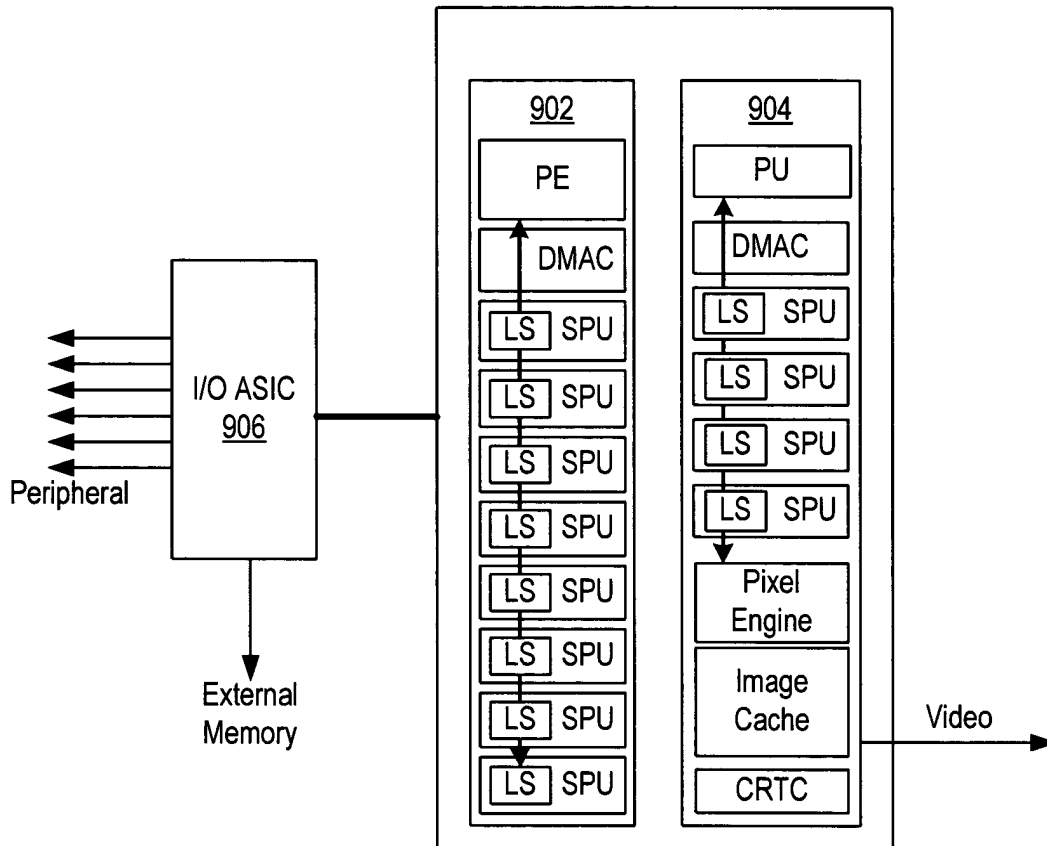
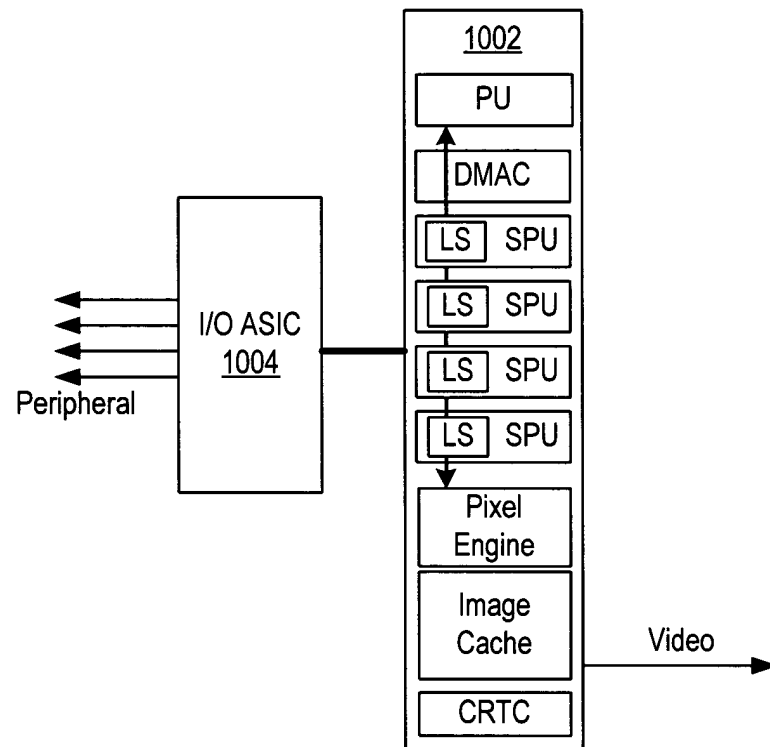
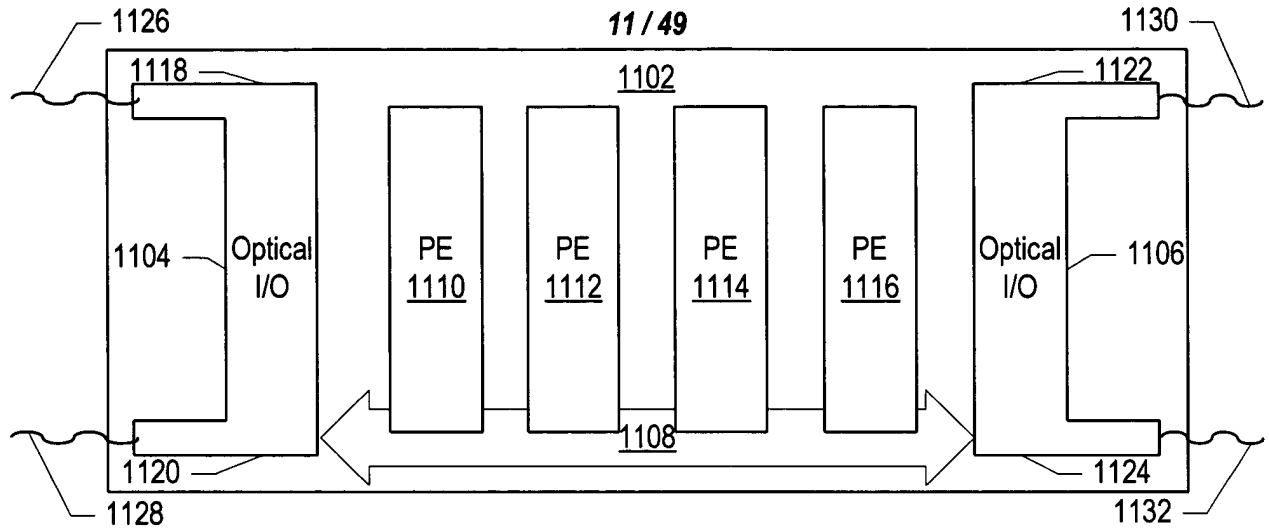
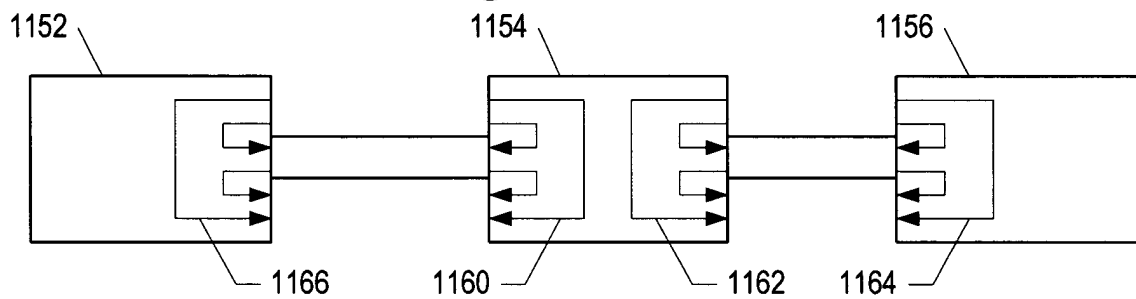
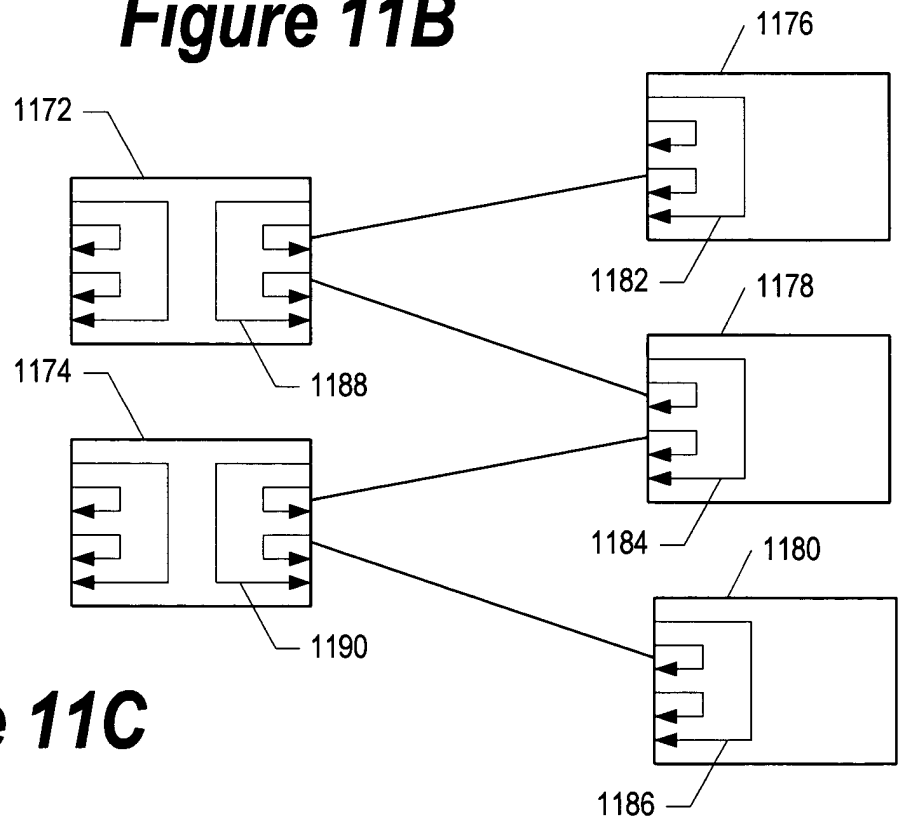


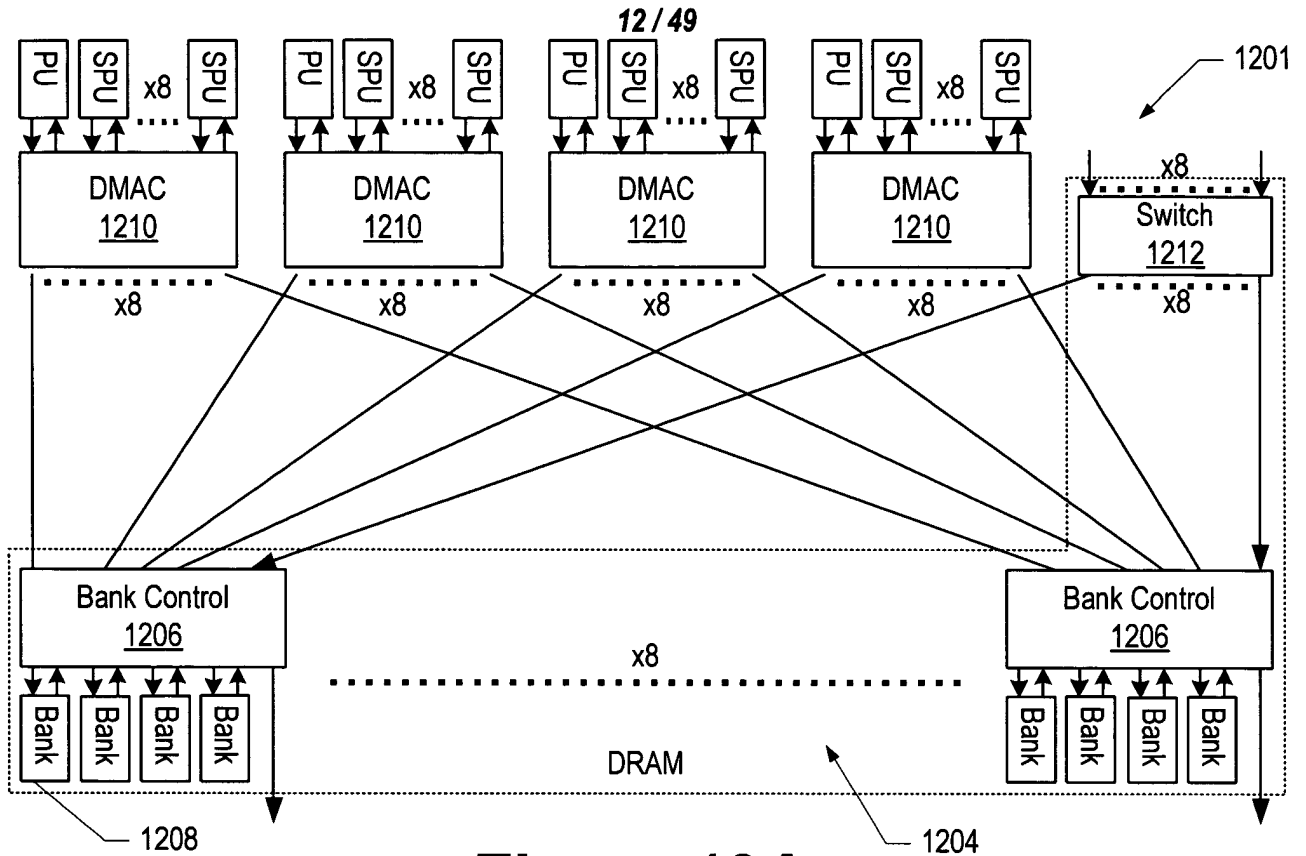
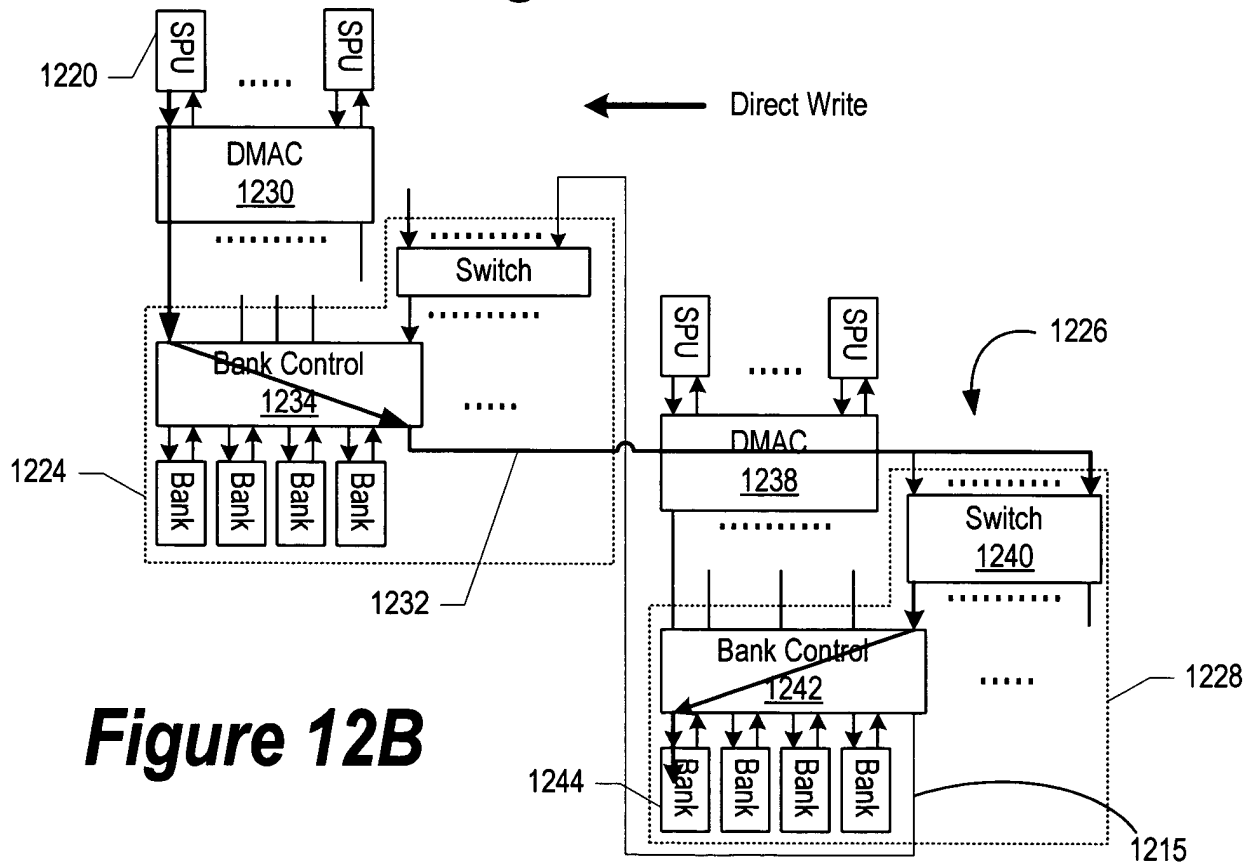
Figure 8

**Figure 9**

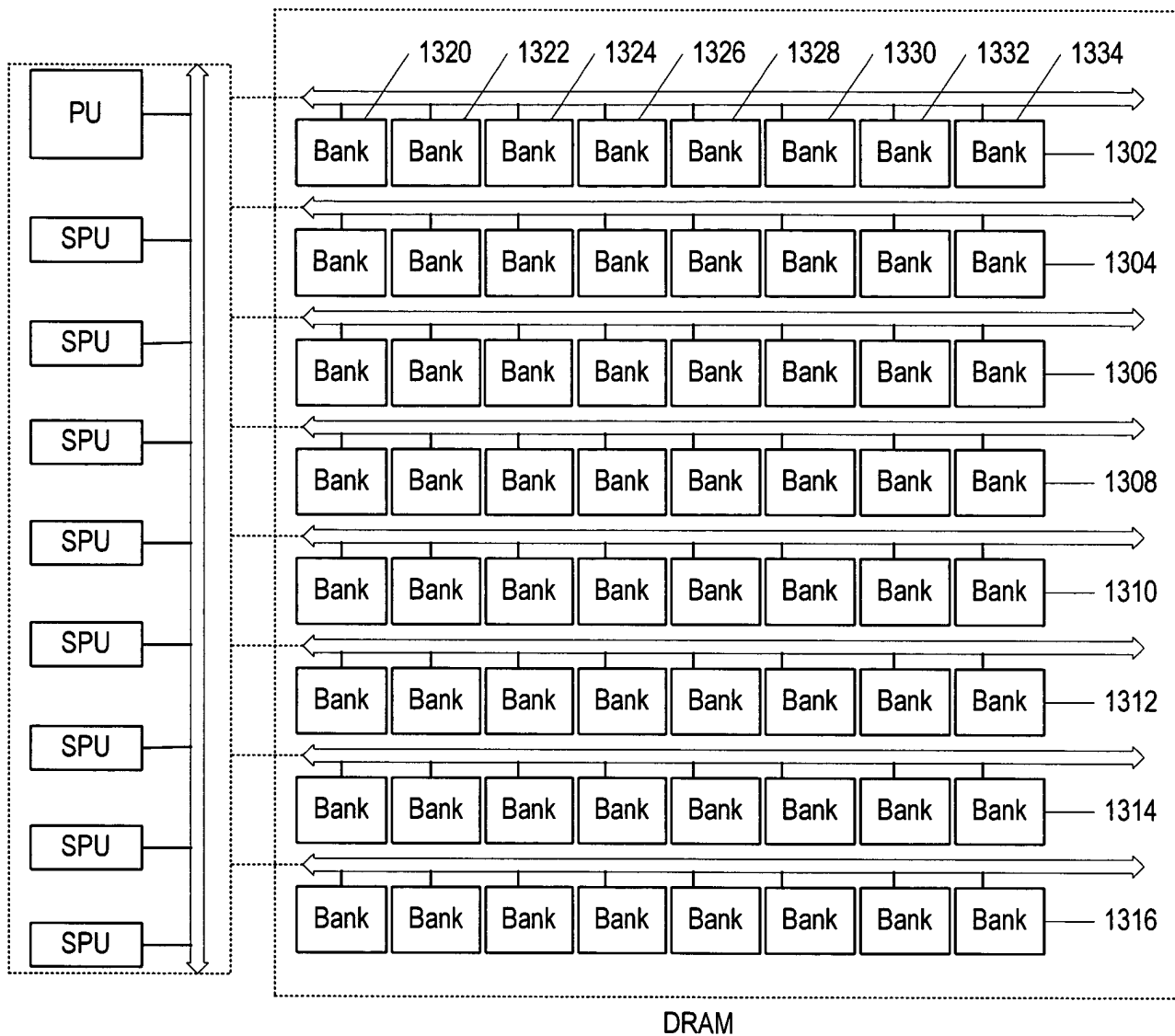
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**Figure 10**

**Figure 11A****Figure 11B****Figure 11C**

**Figure 12A****Figure 12B**

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**Figure 13**

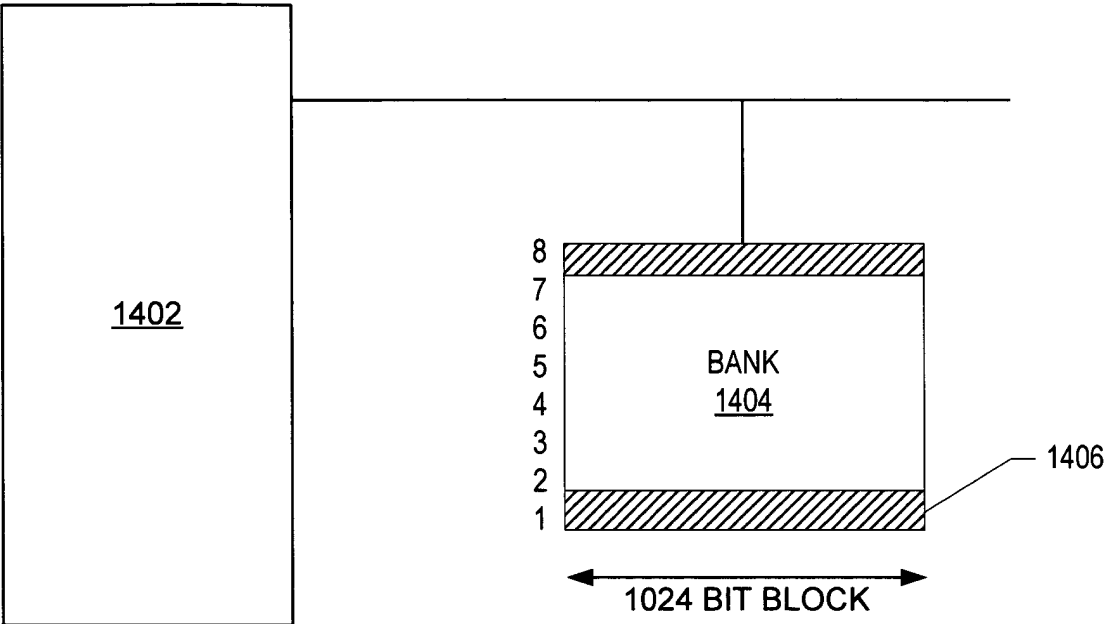


Figure 14A

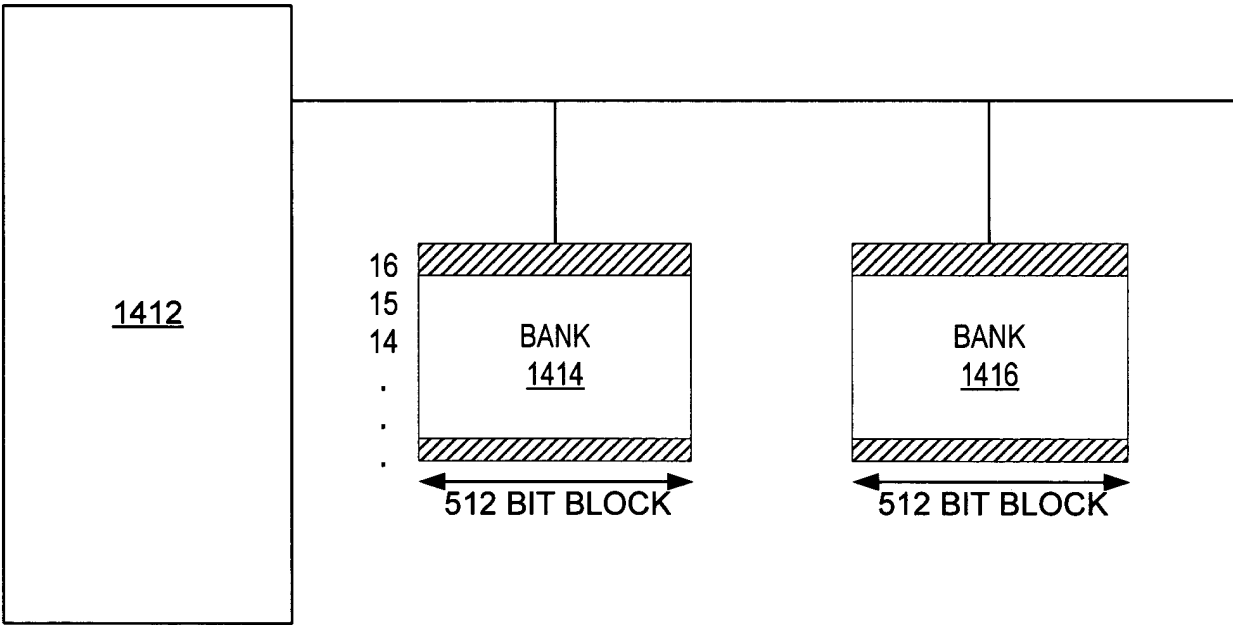
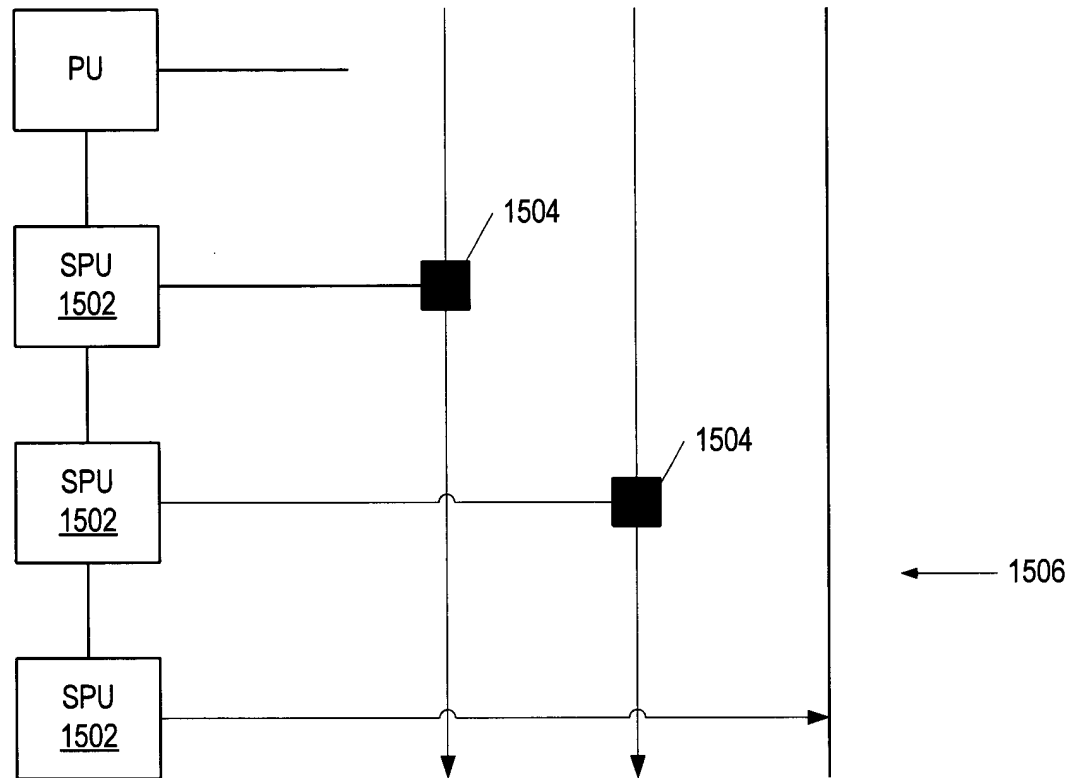


Figure 14B

**Figure 15**

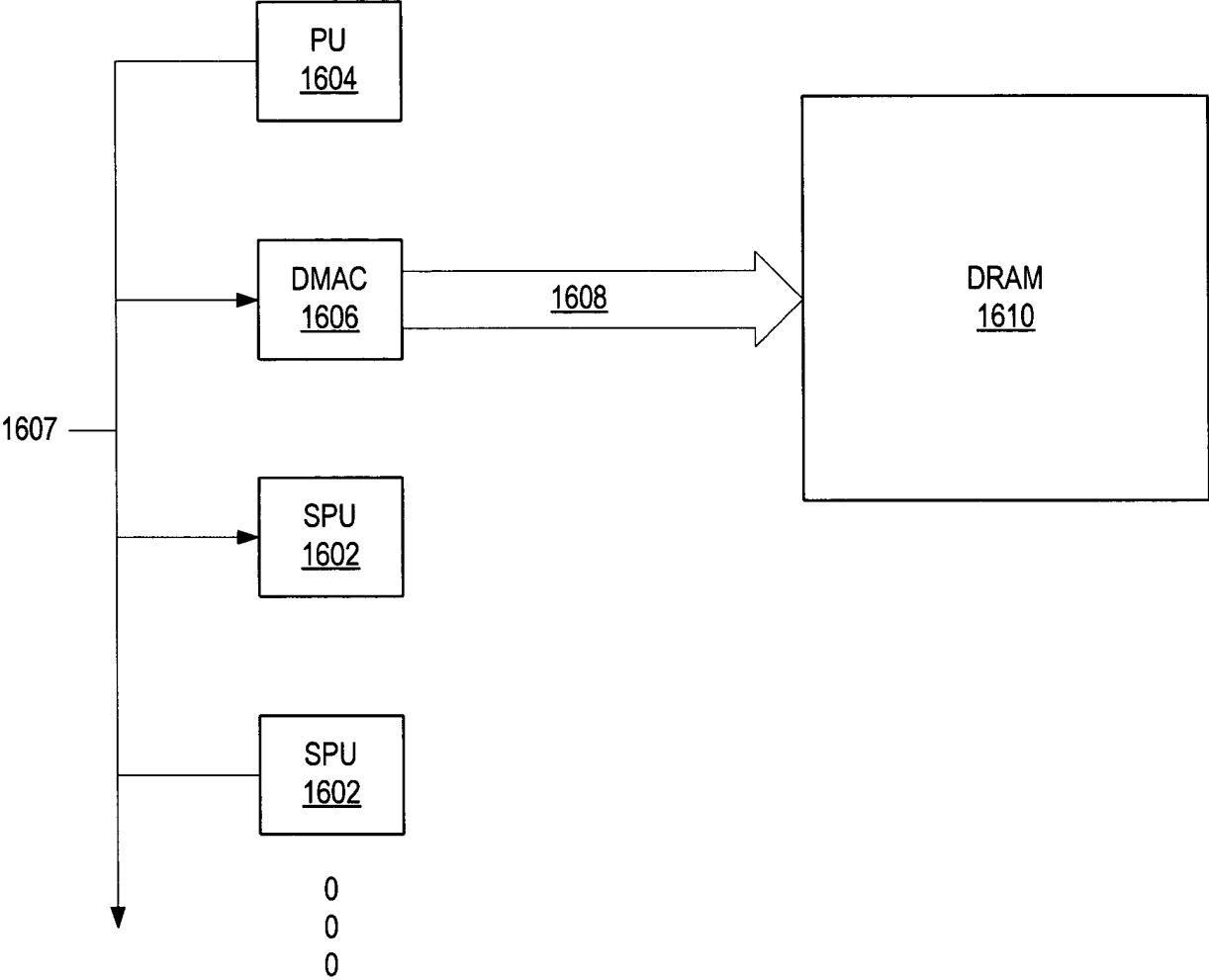


Figure 16

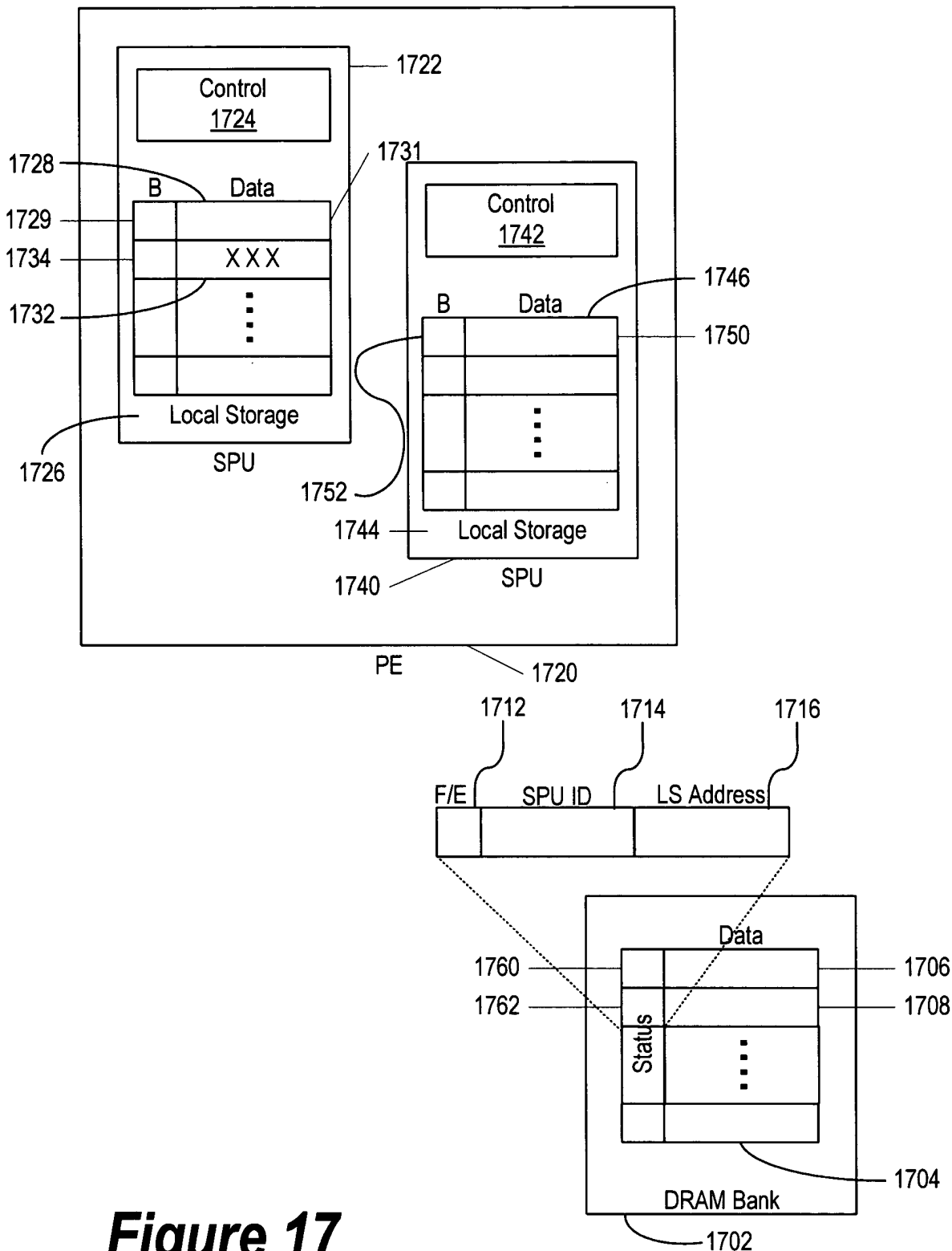


Figure 17

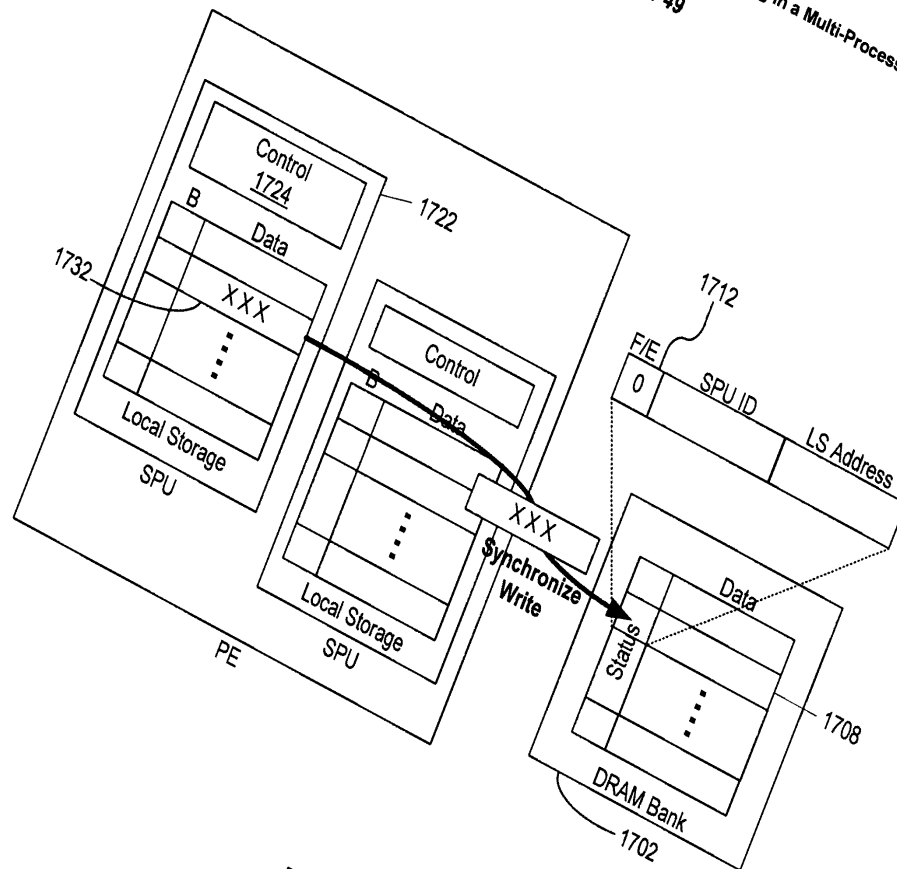


Figure 18

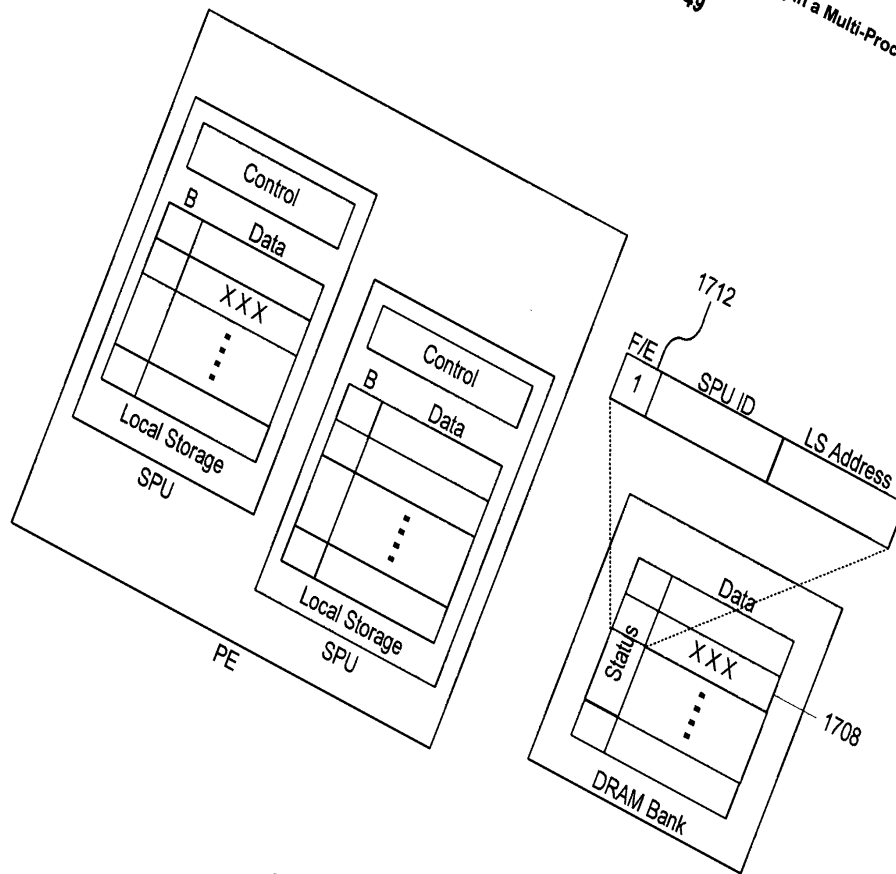
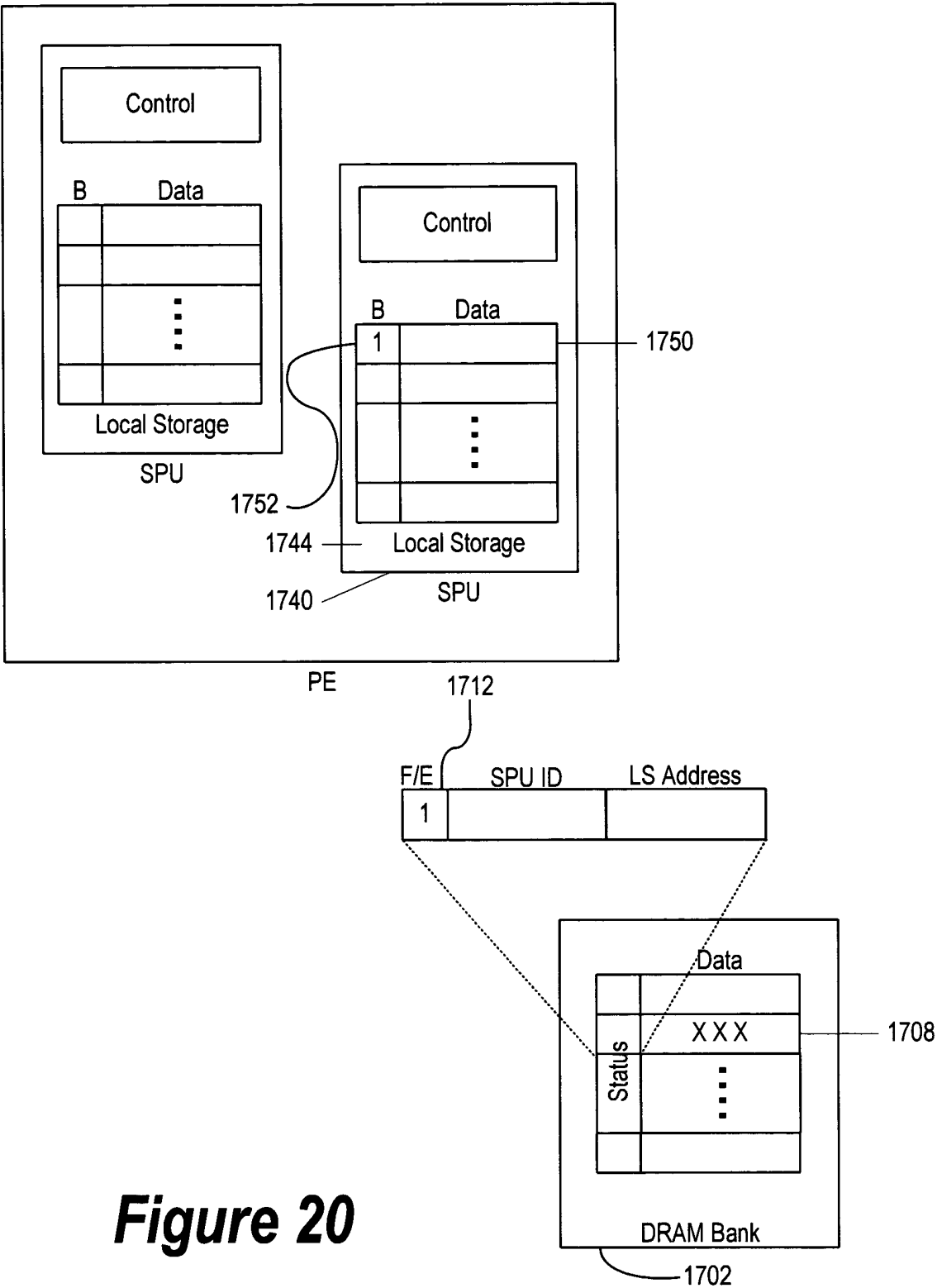


Figure 19



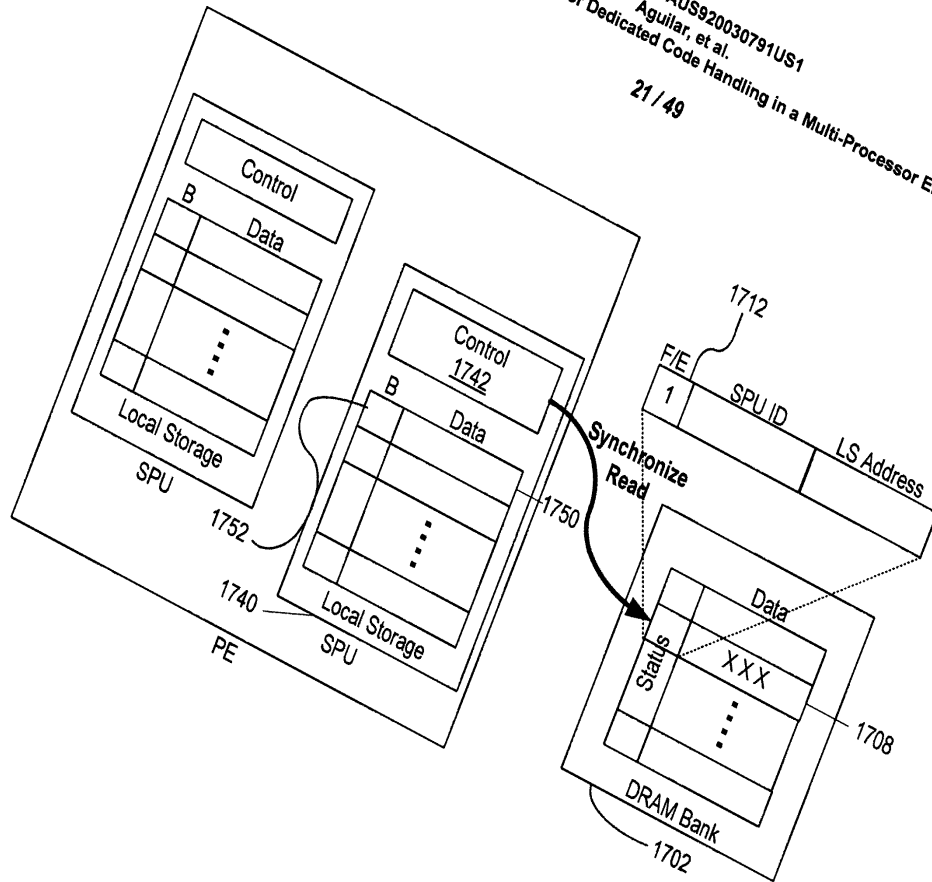


Figure 21

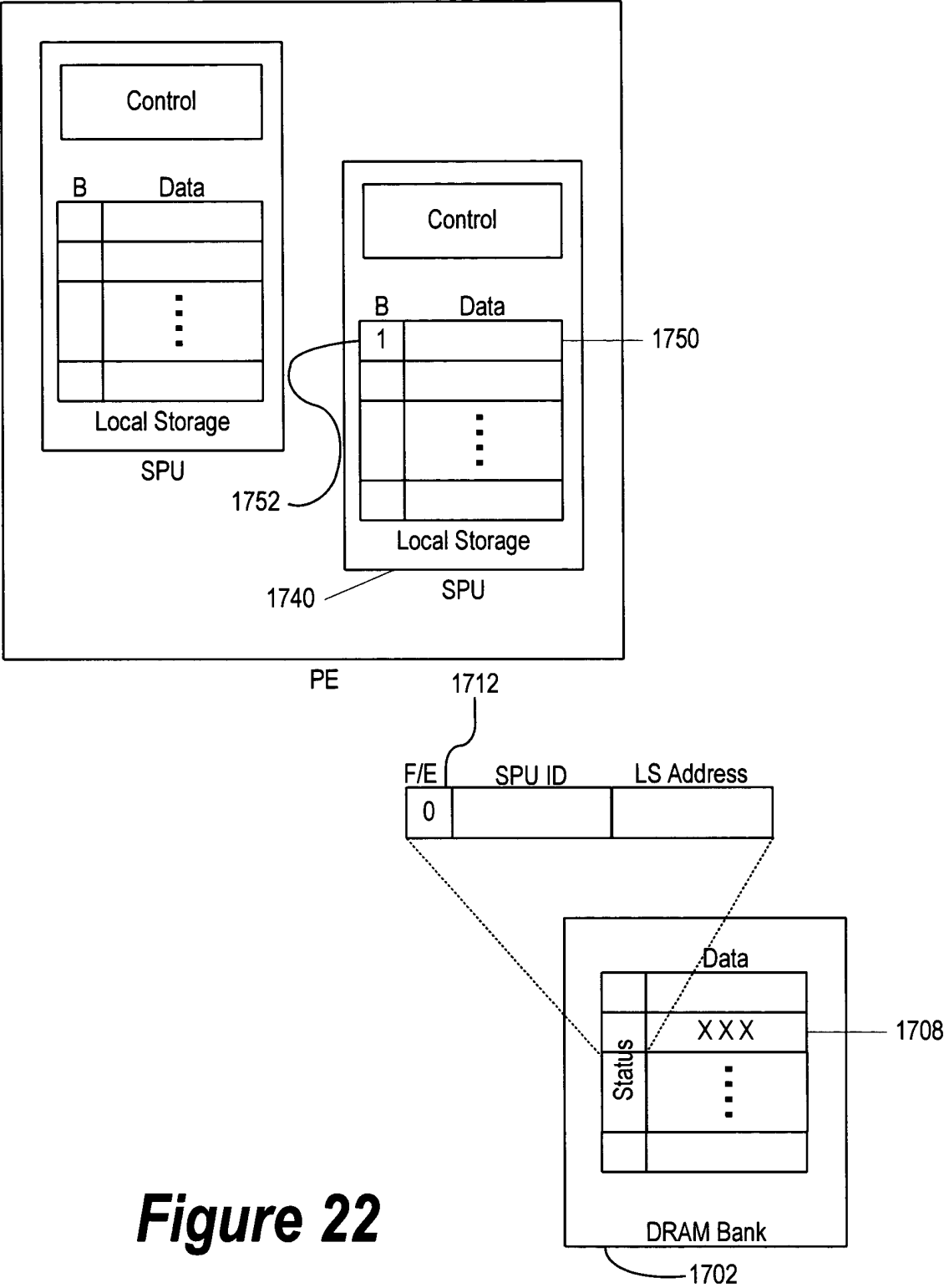


Figure 22

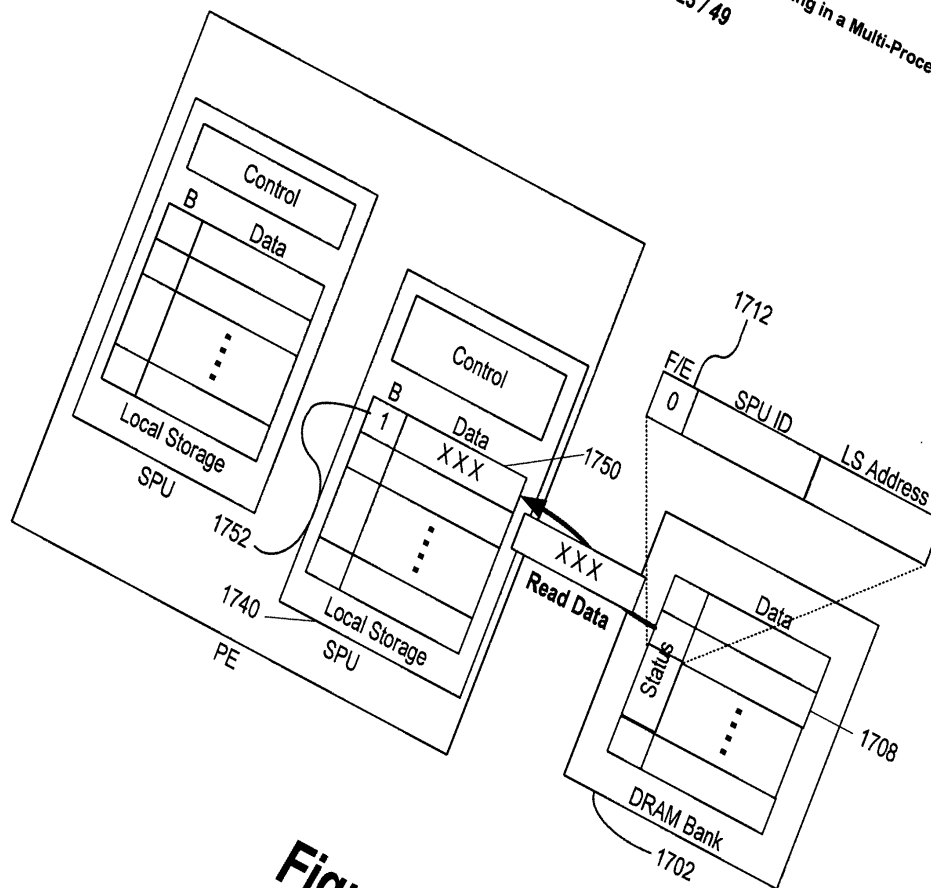


Figure 23

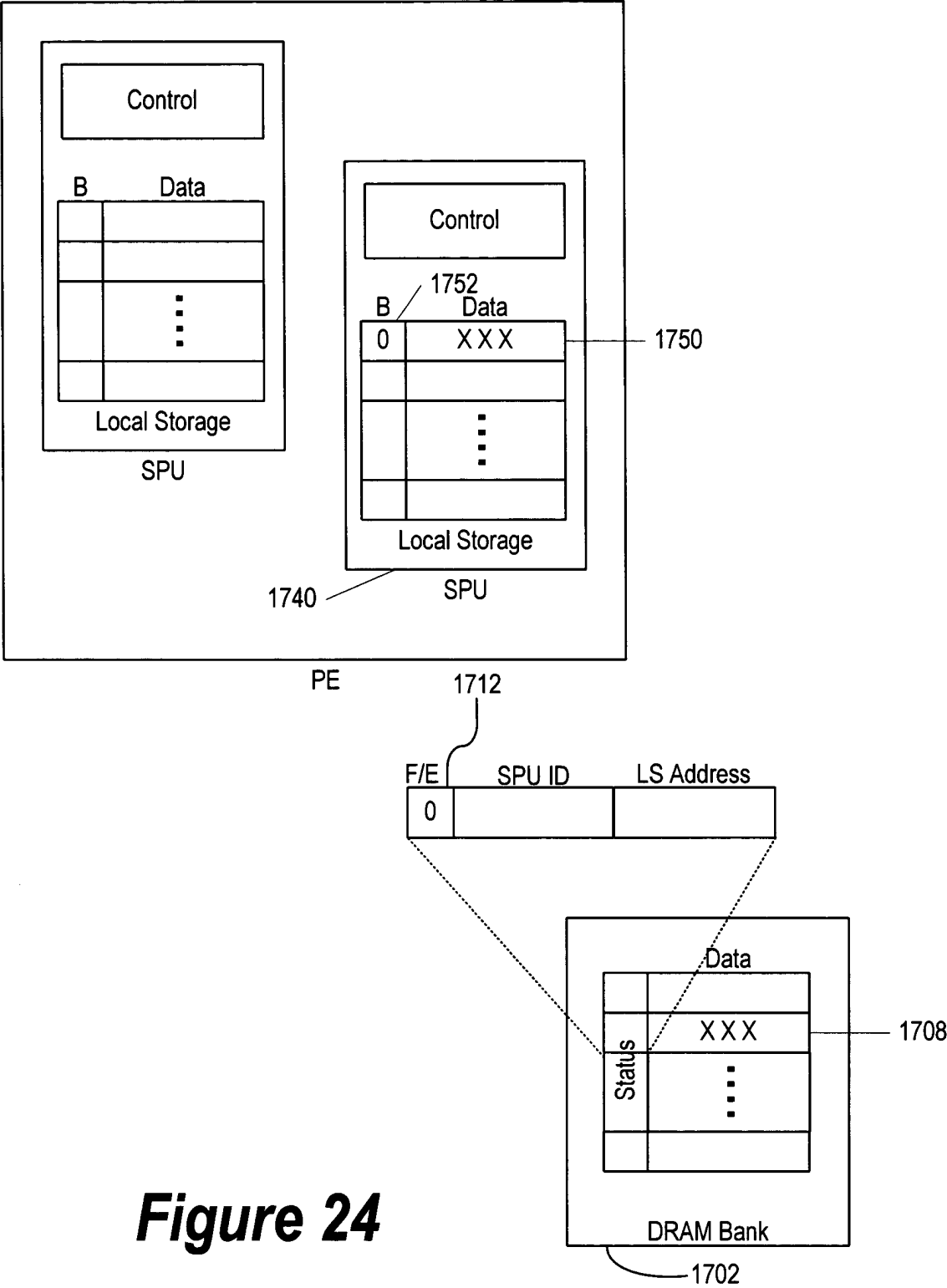


Figure 24

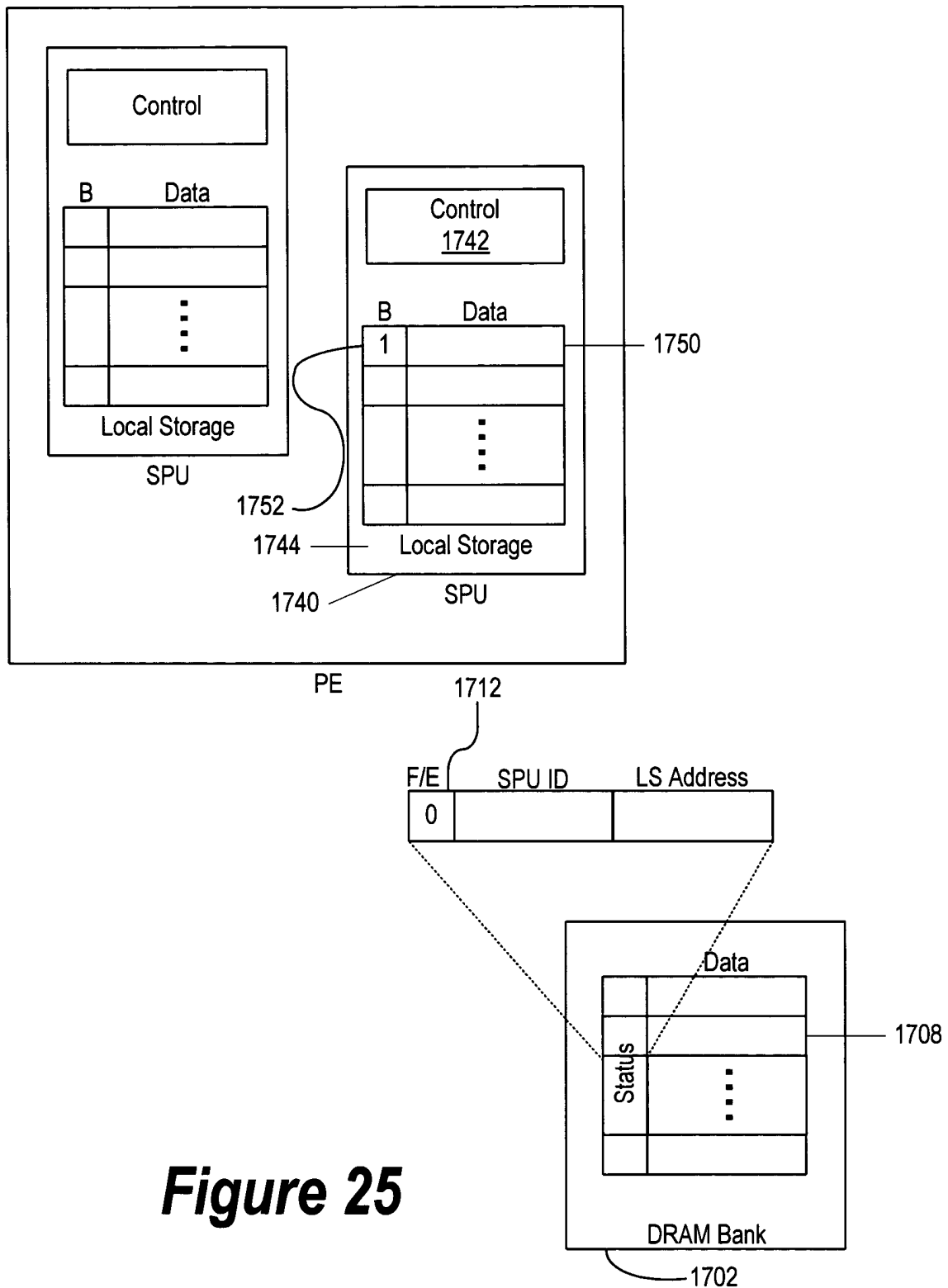


Figure 25

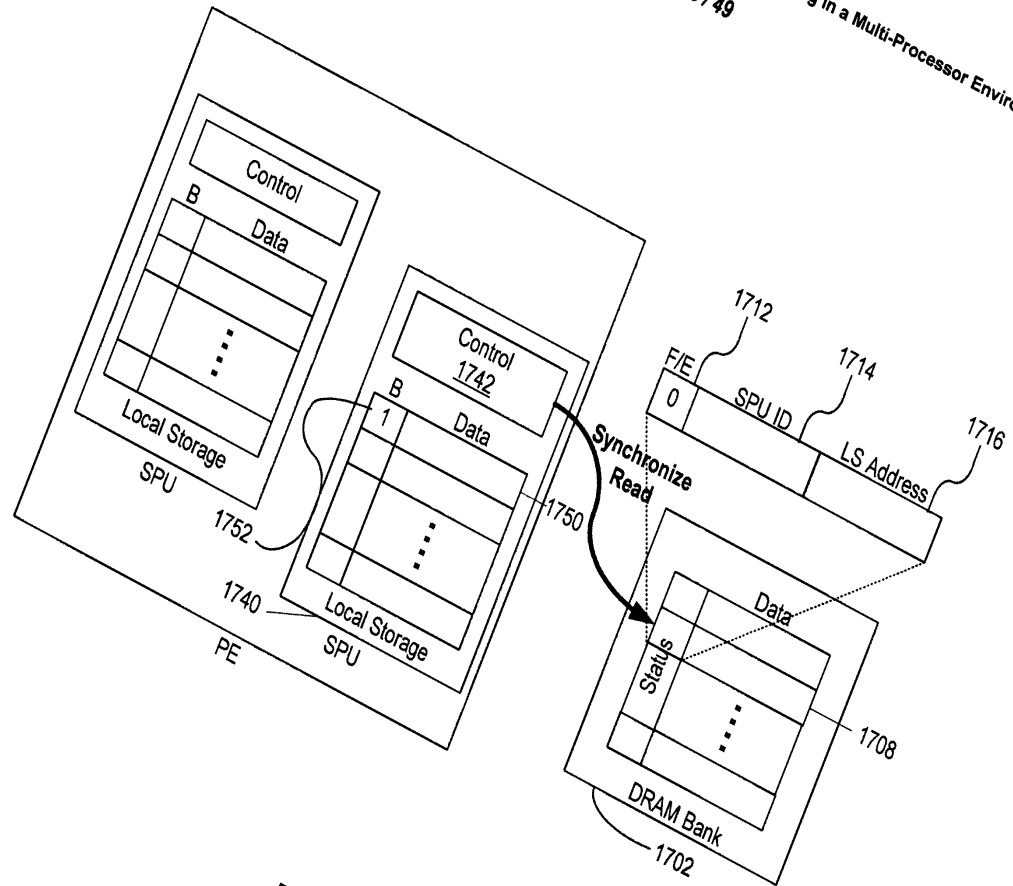


Figure 26

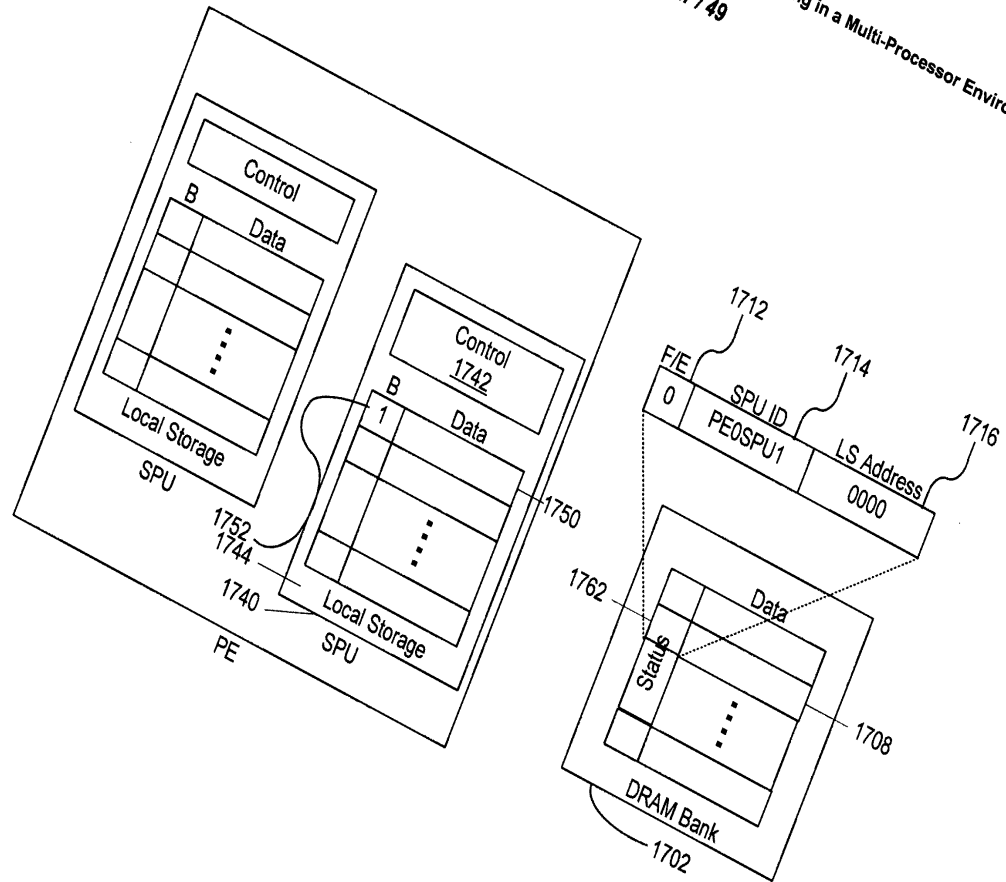


Figure 27

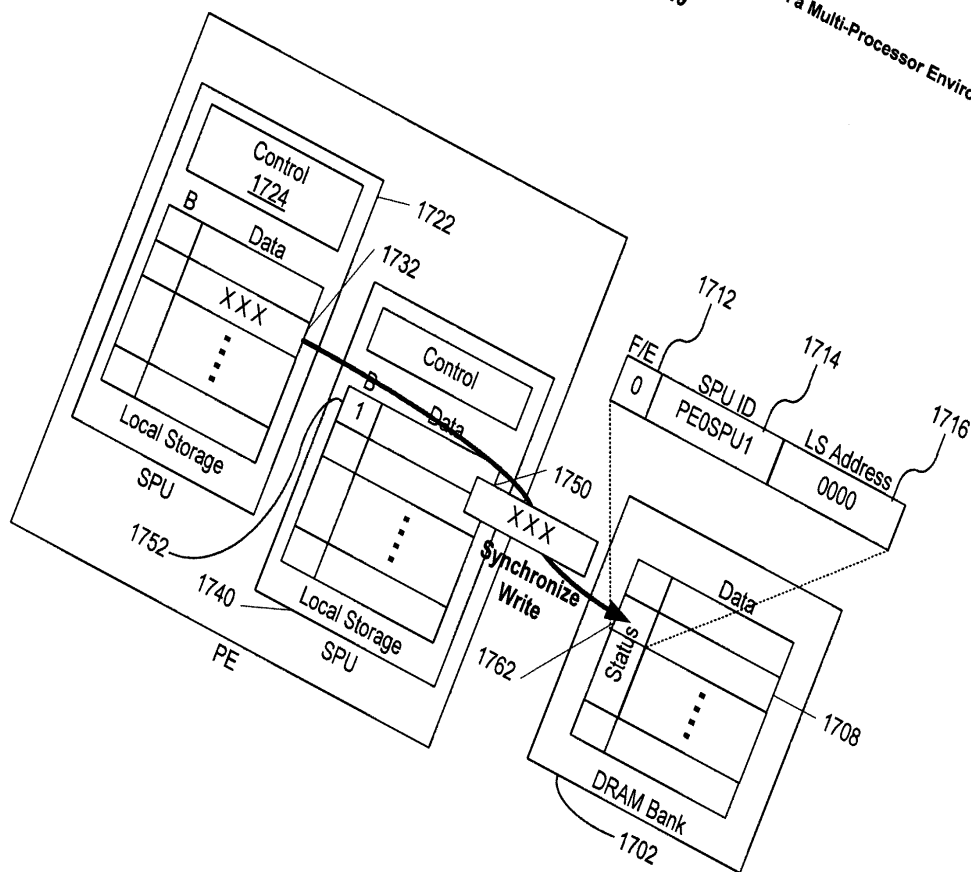


Figure 28

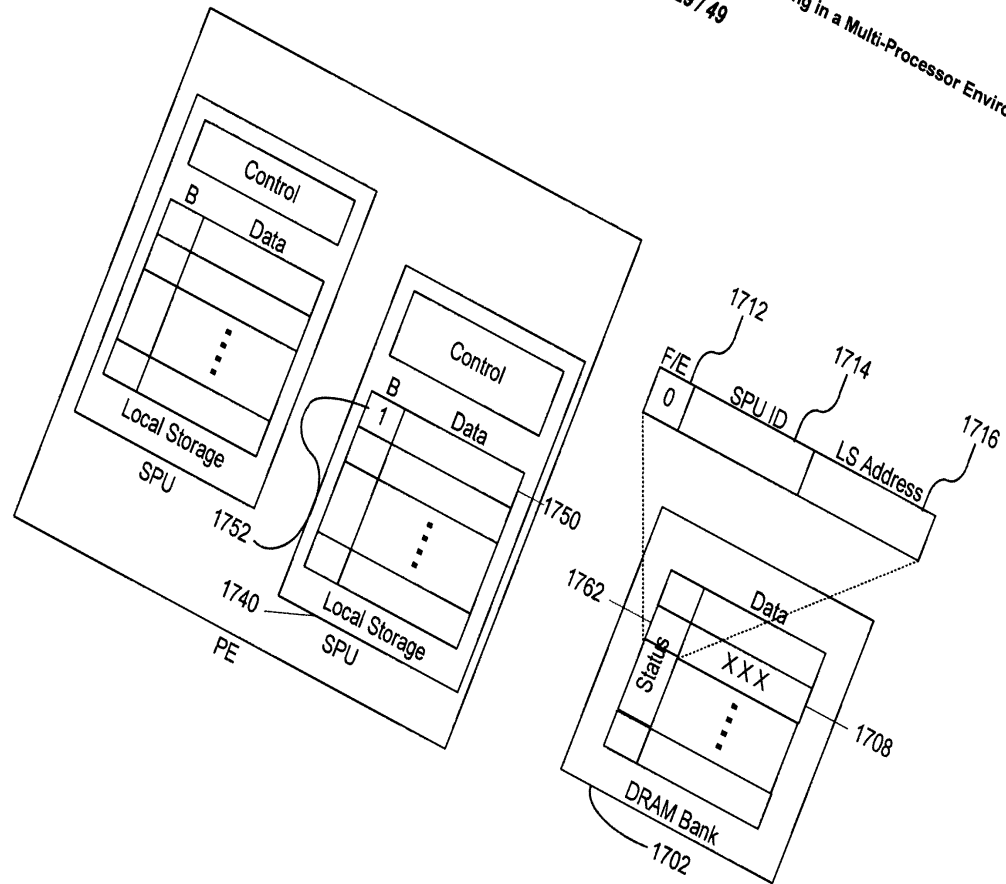


Figure 29

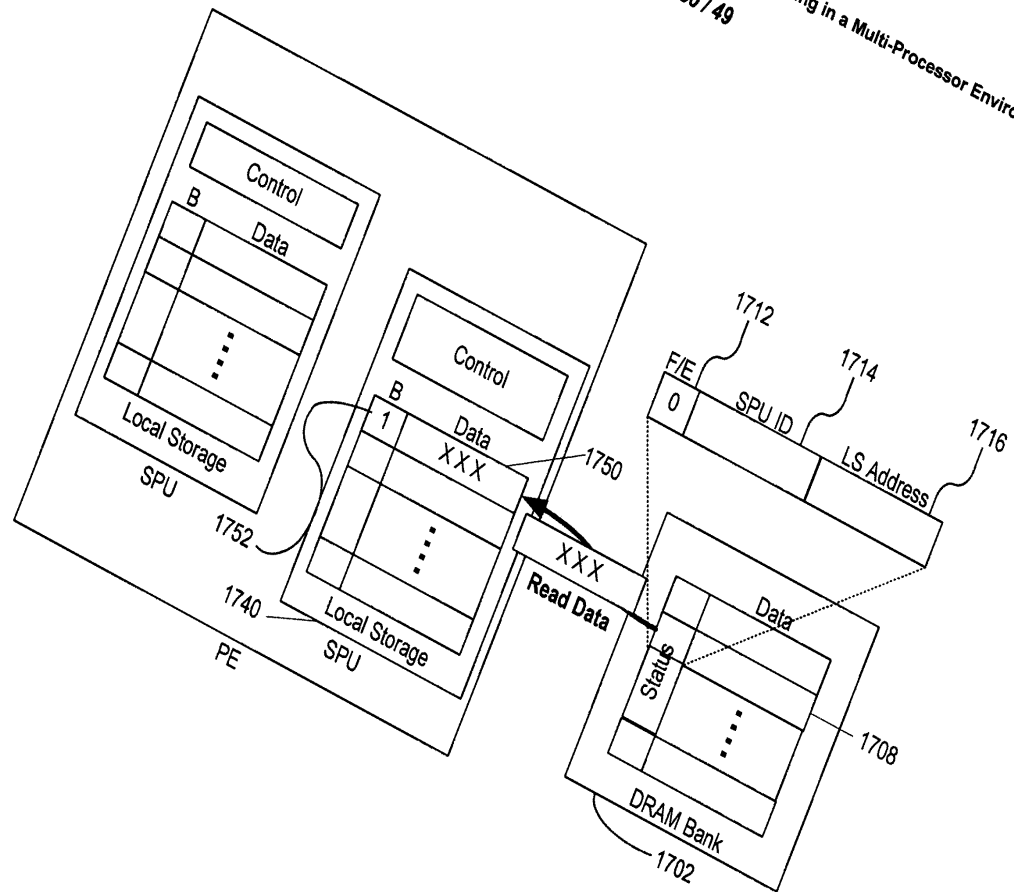


Figure 30

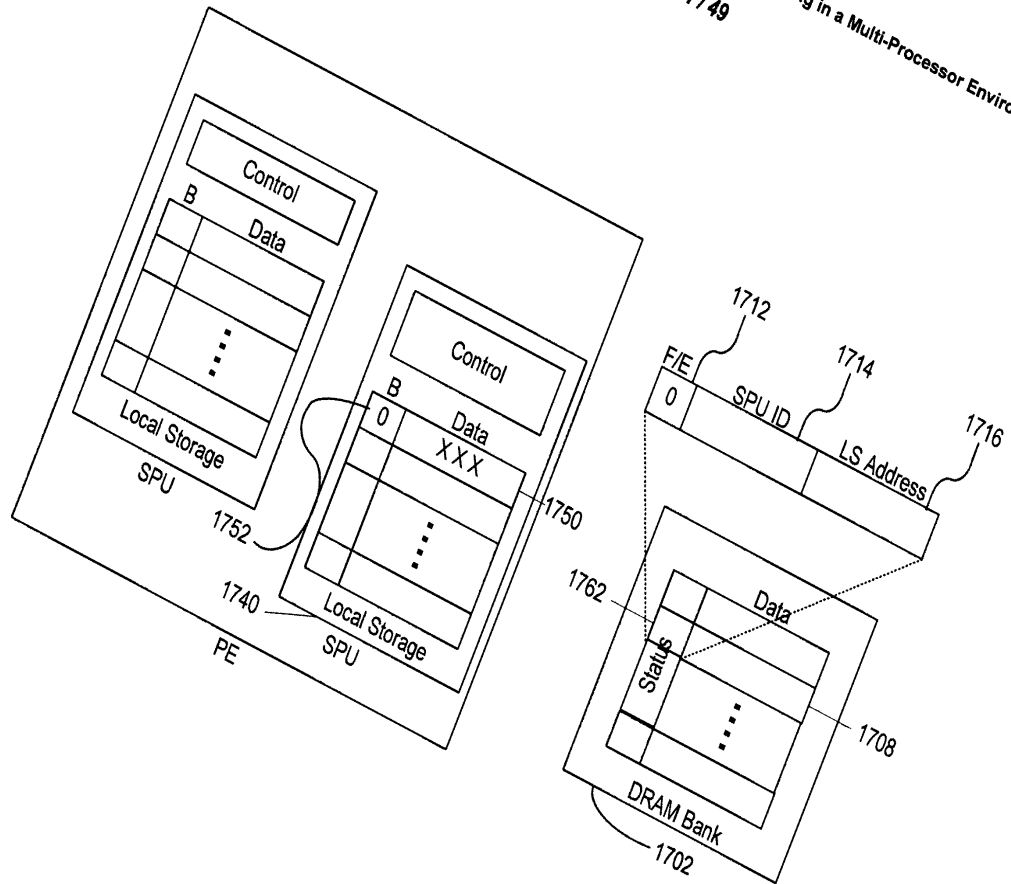


Figure 31

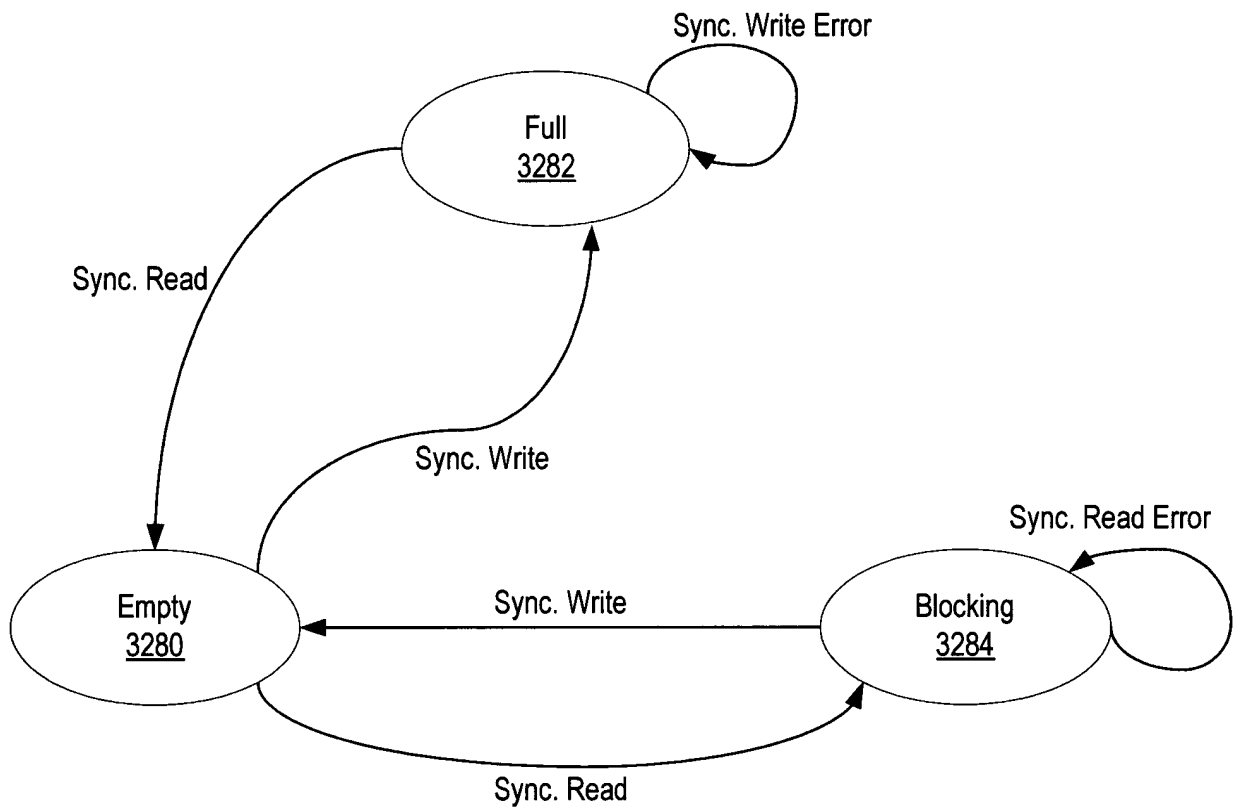


Figure 32

Key Control Table

3302

3304	ID	3306	3308
0	SPU Key	Key Mask	
1	SPU Key	Key Mask	
2	SPU Key	Key Mask	
		⋮	
7	SPU Key	Key Mask	

Figure 33

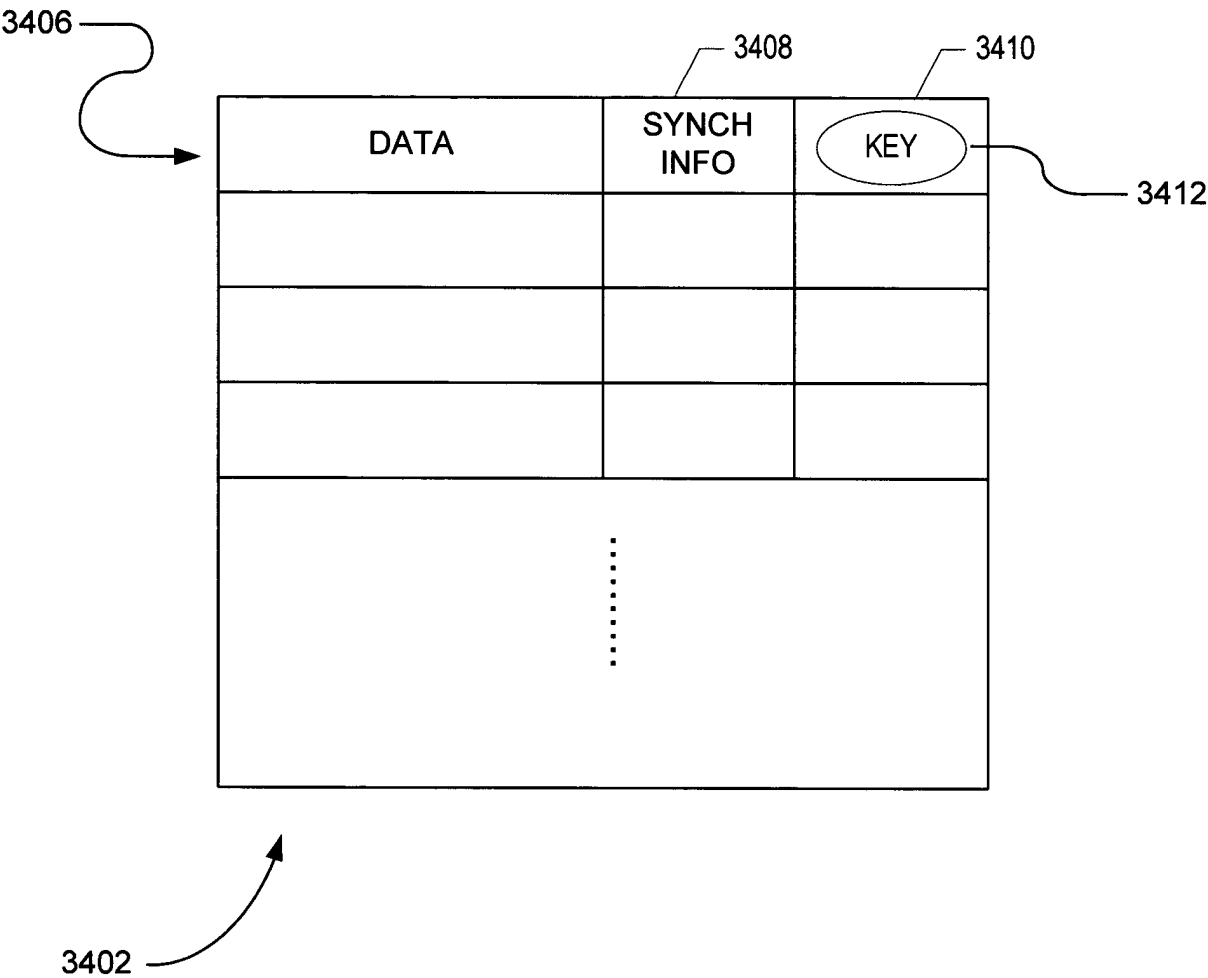


Figure 34

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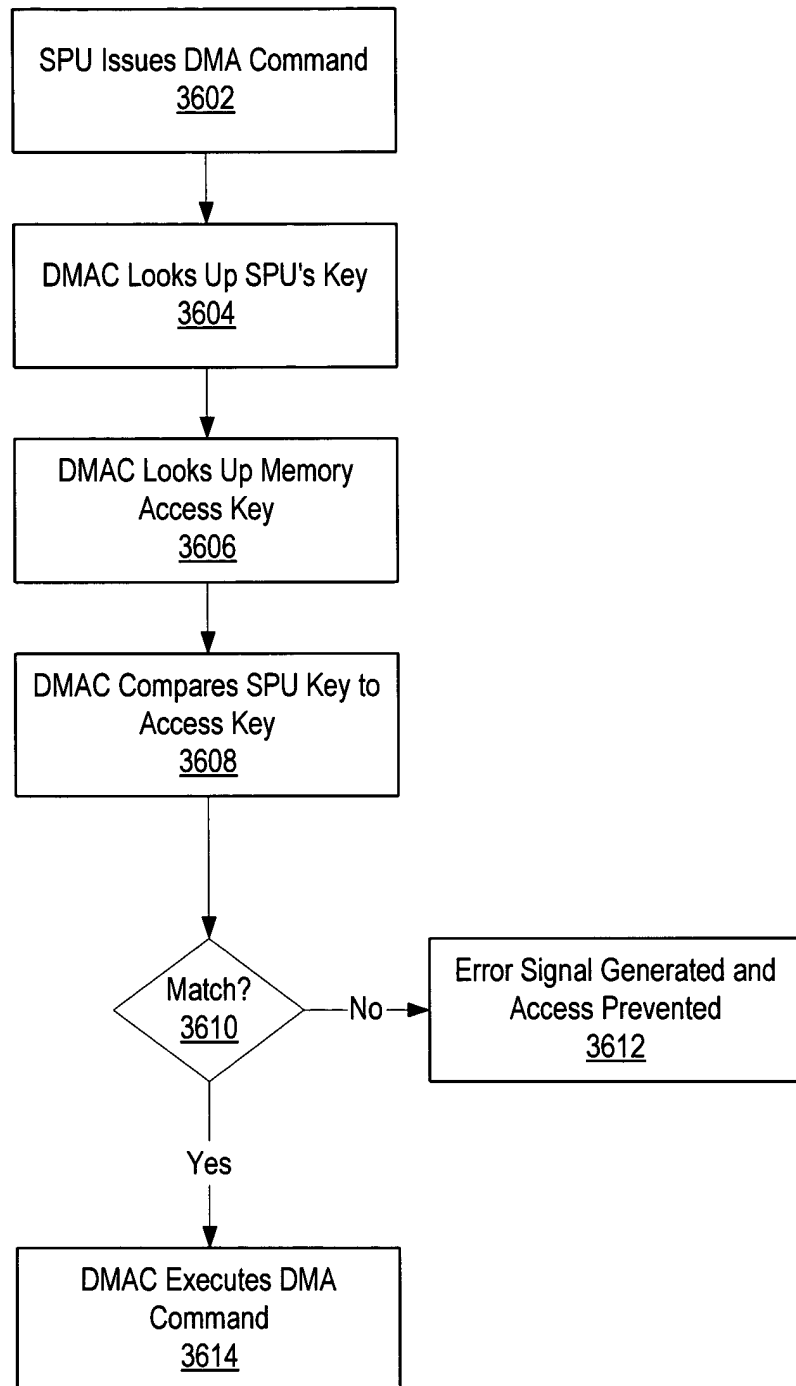


Figure 36

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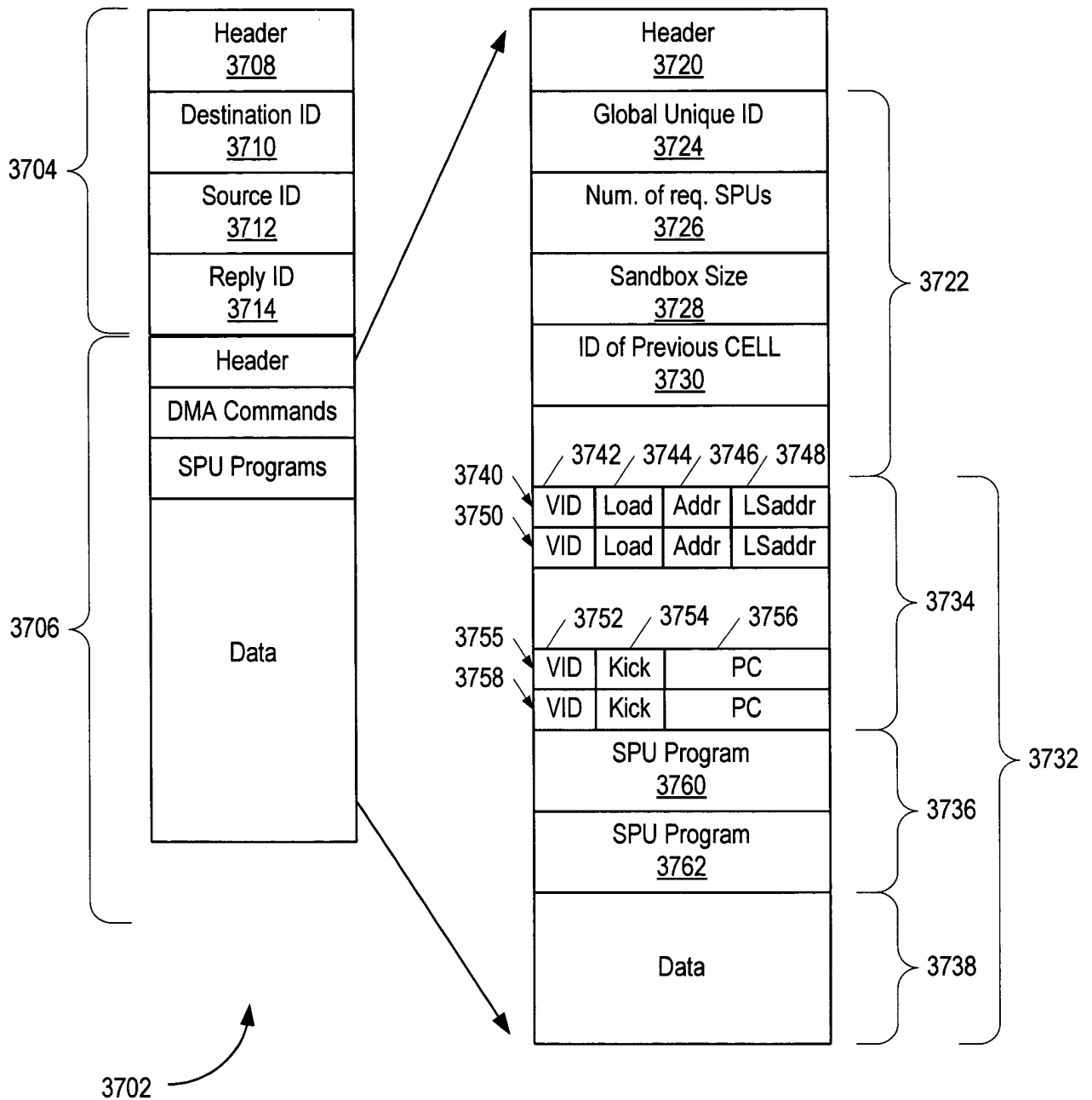


Figure 37

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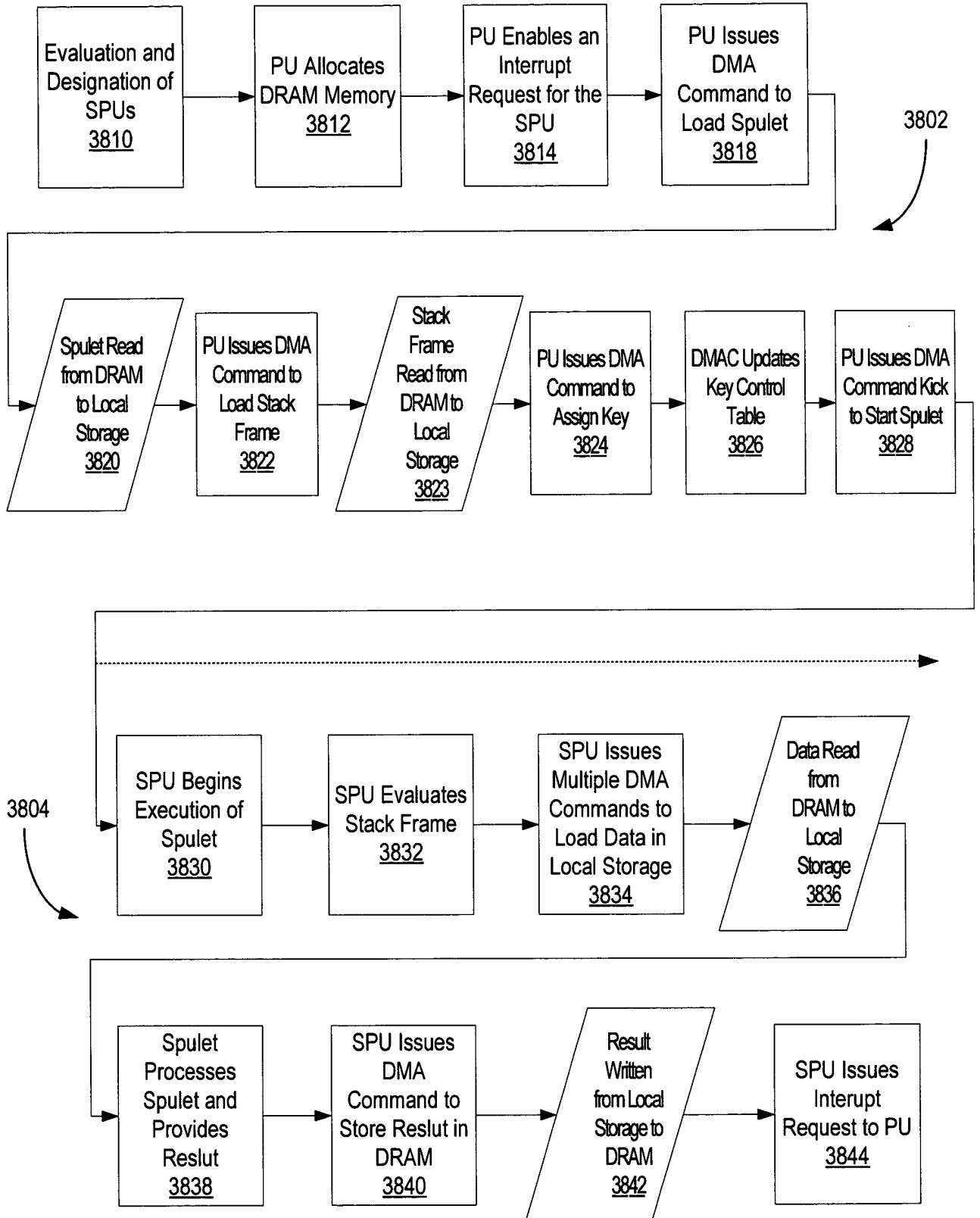
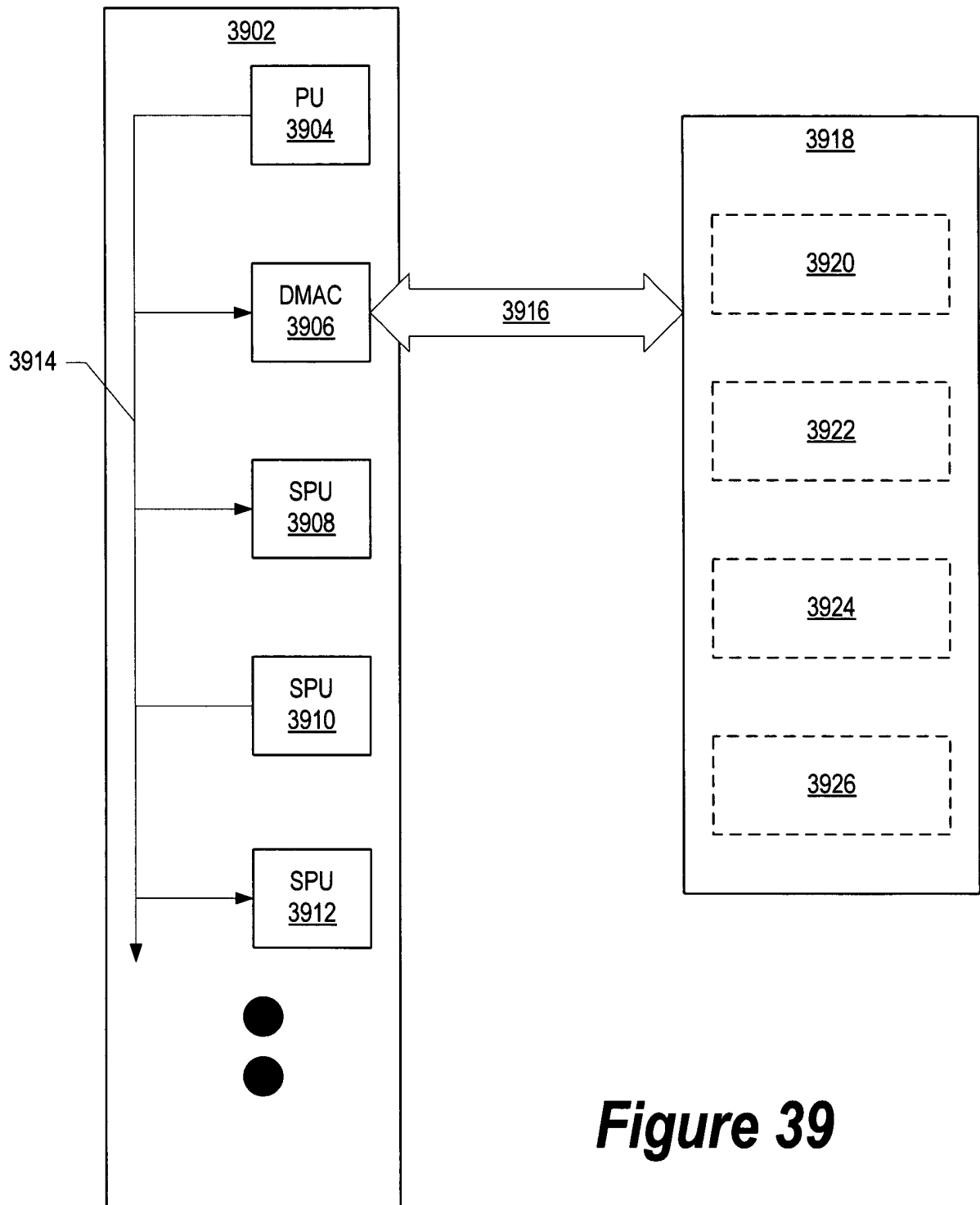


Figure 38

**Figure 39**

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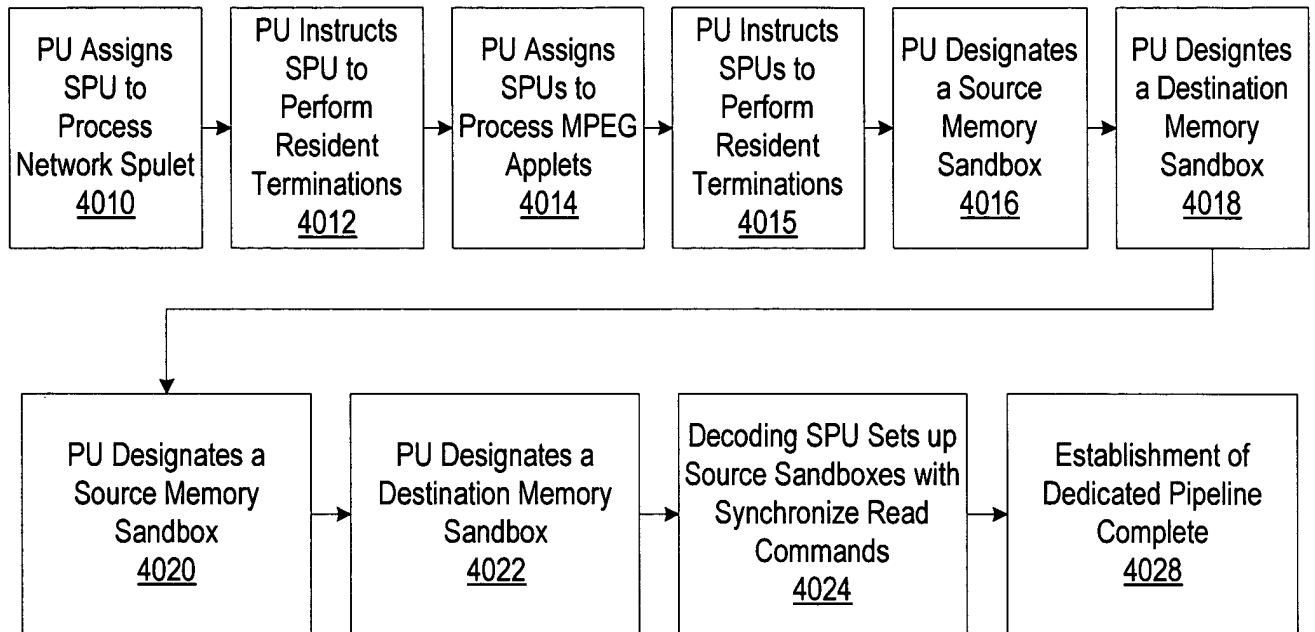


Figure 40A

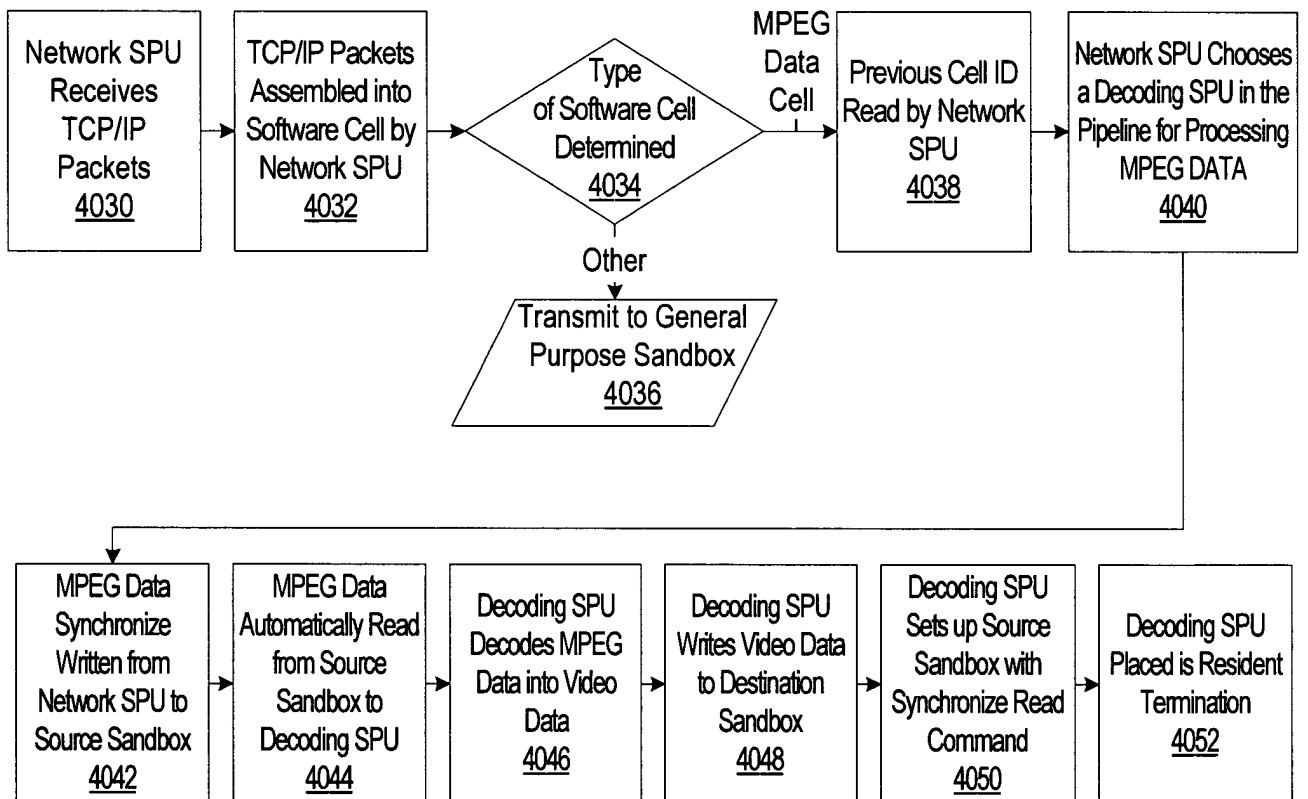
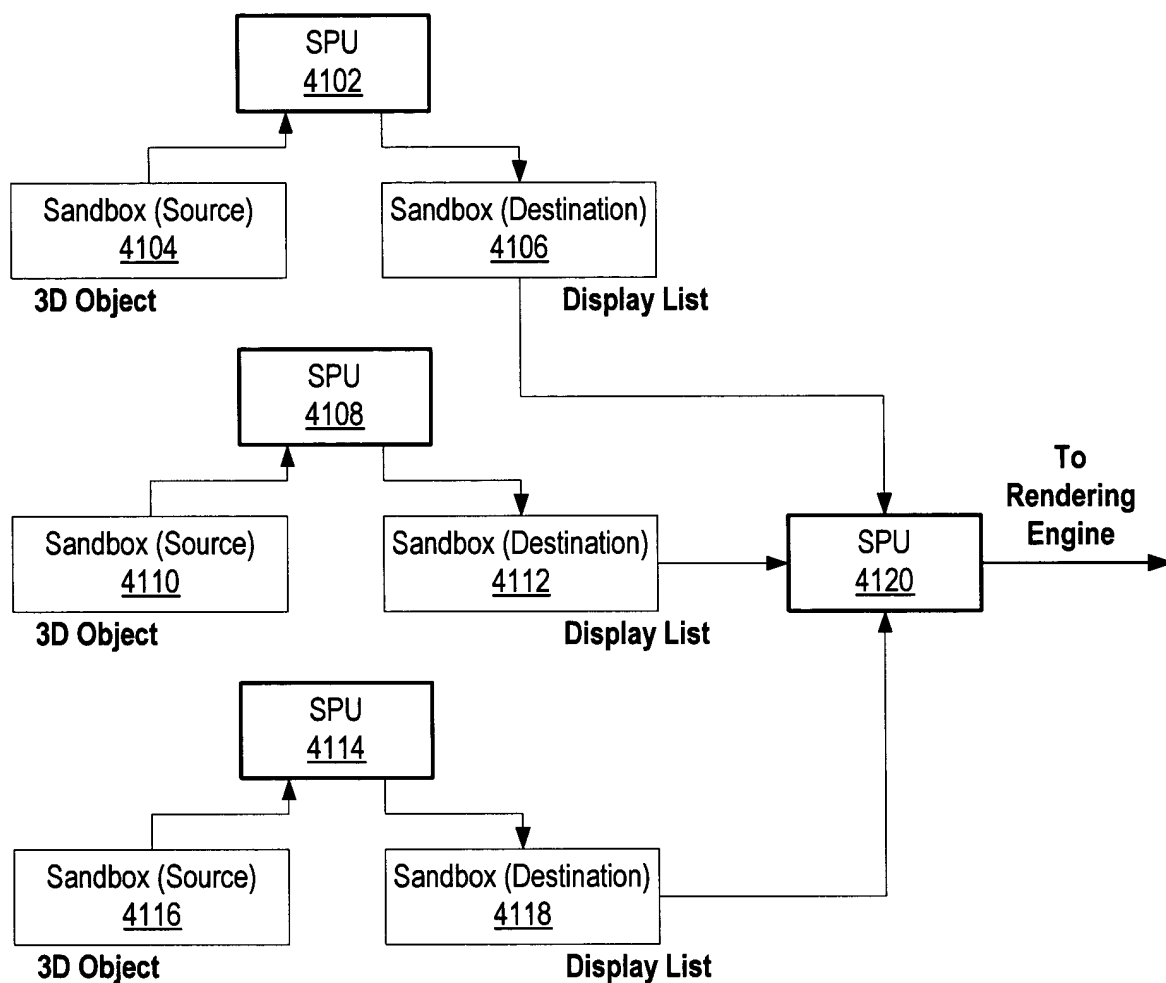
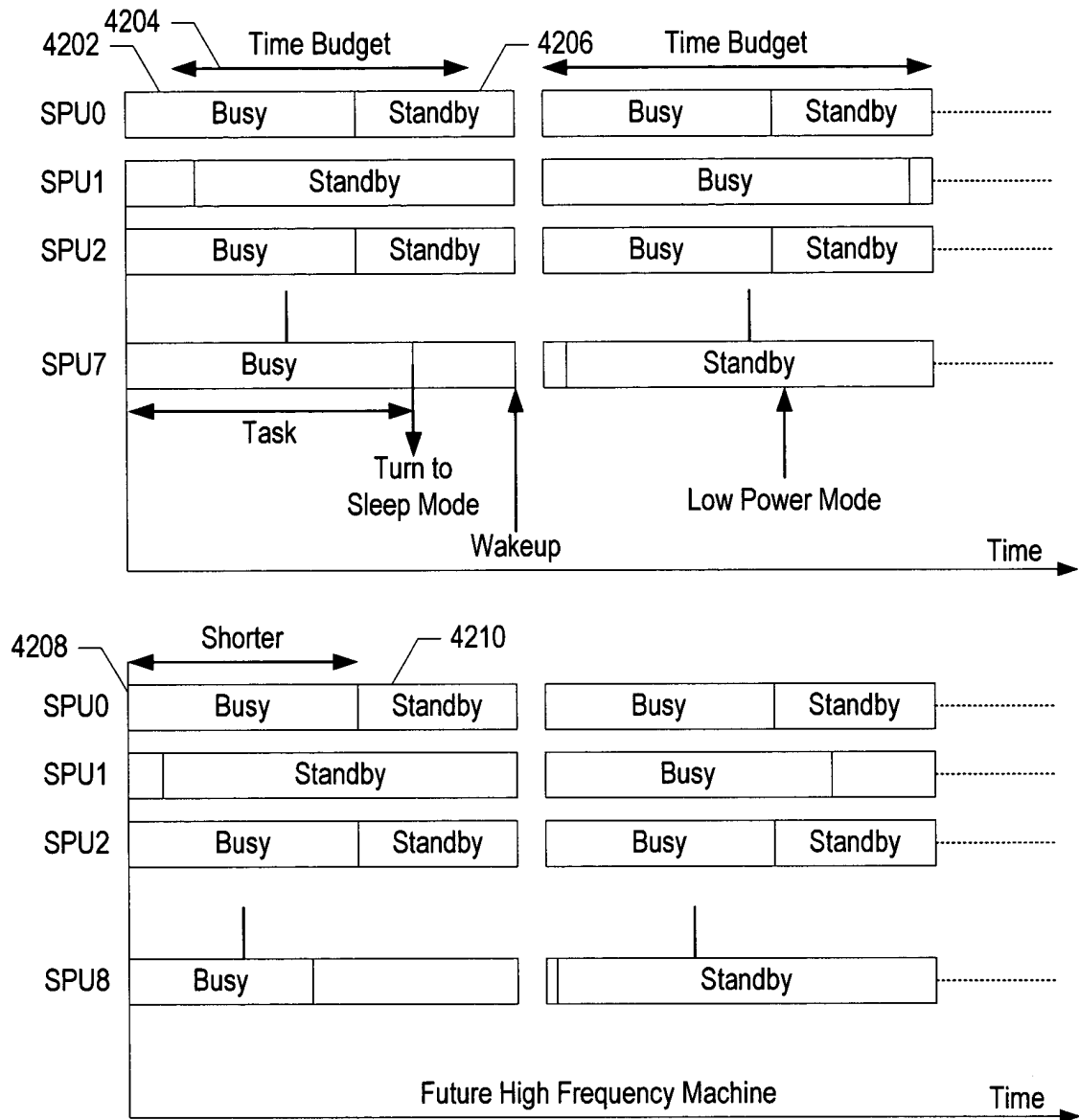


Figure 40B

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**Figure 41**

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**Figure 42**

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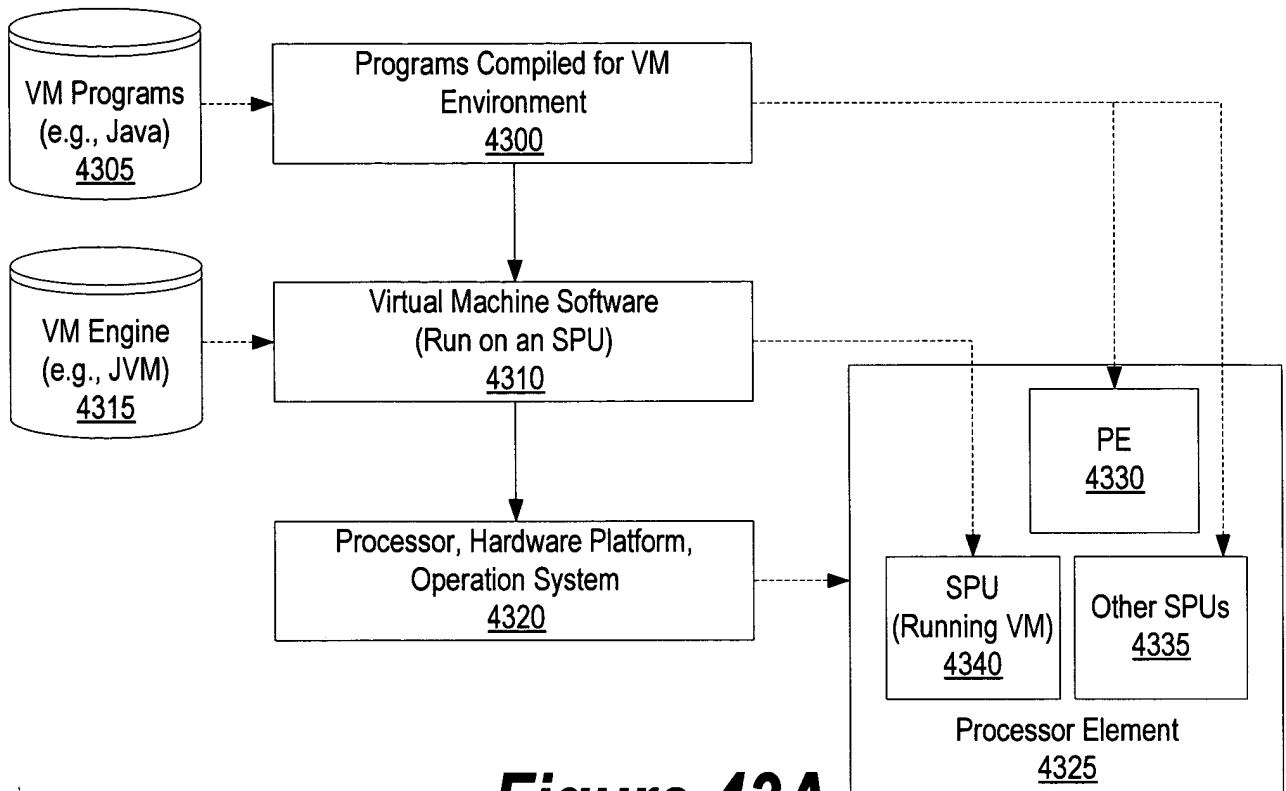


Figure 43A

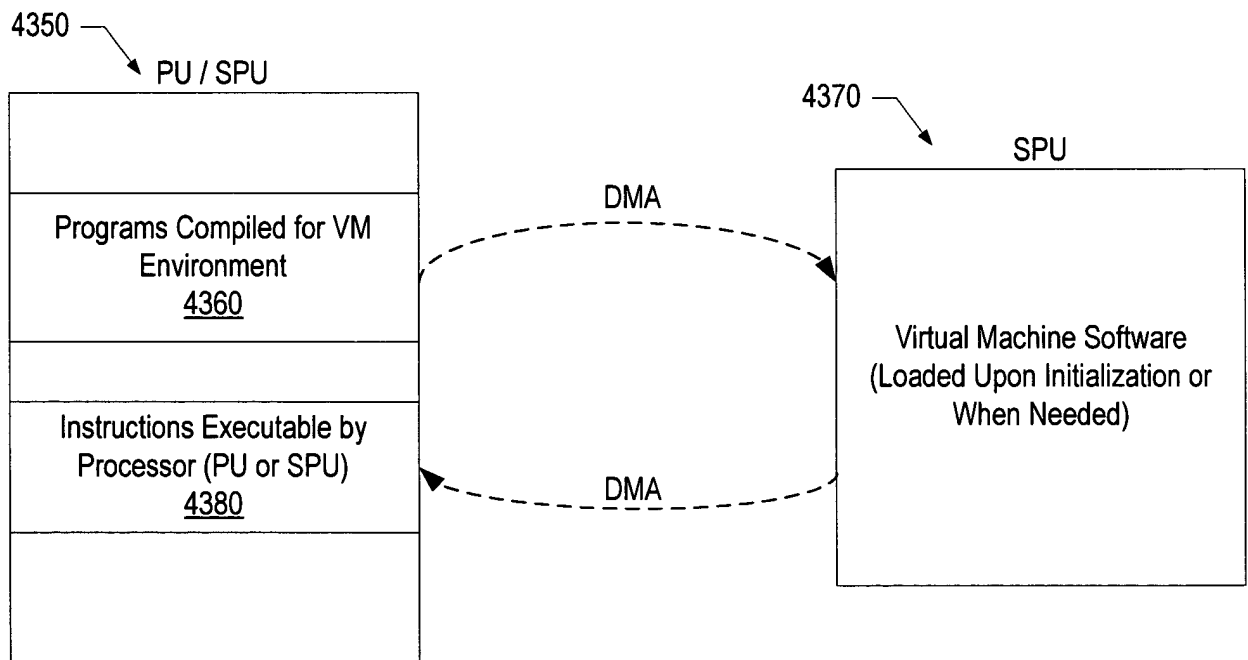


Figure 43B

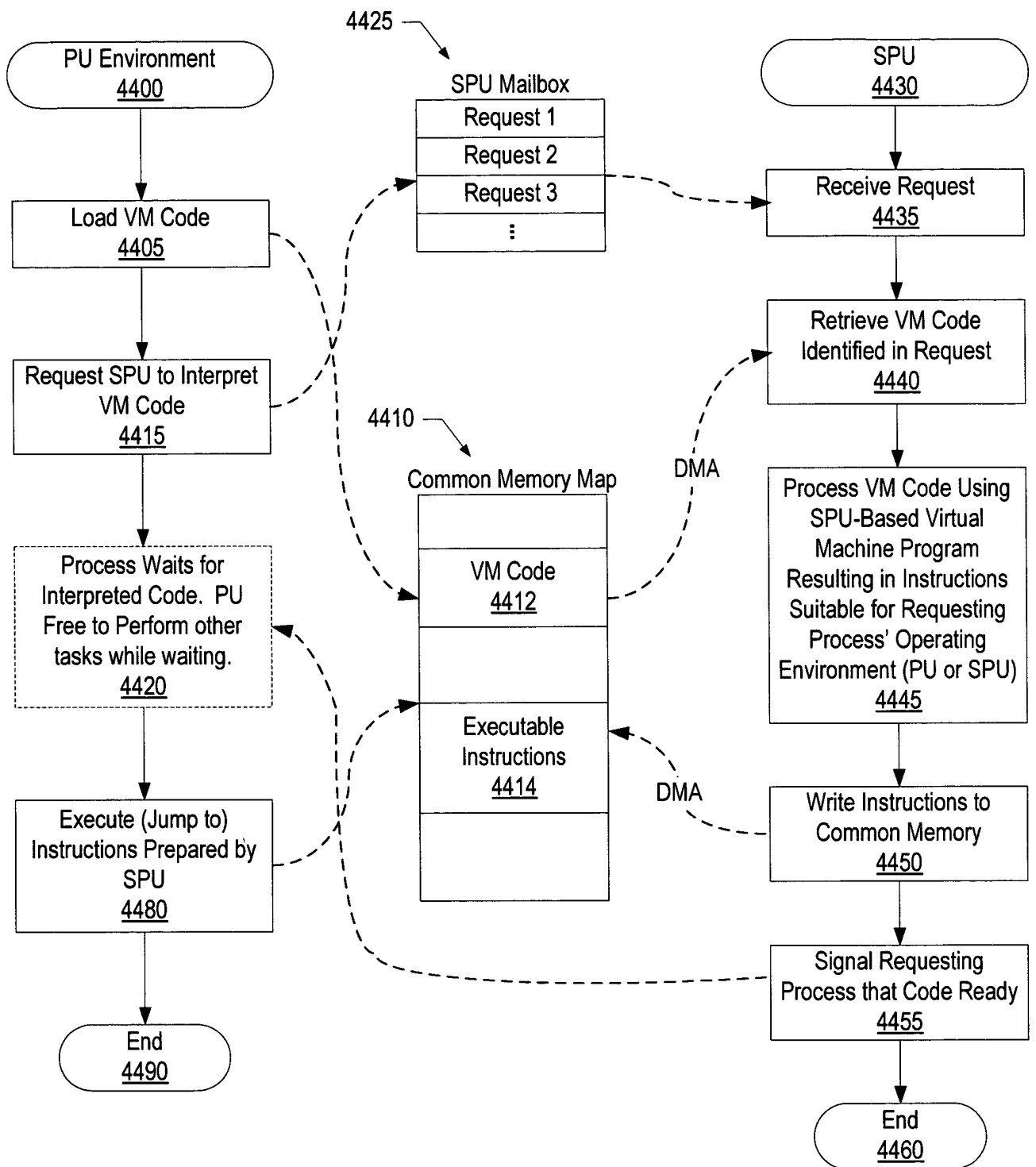
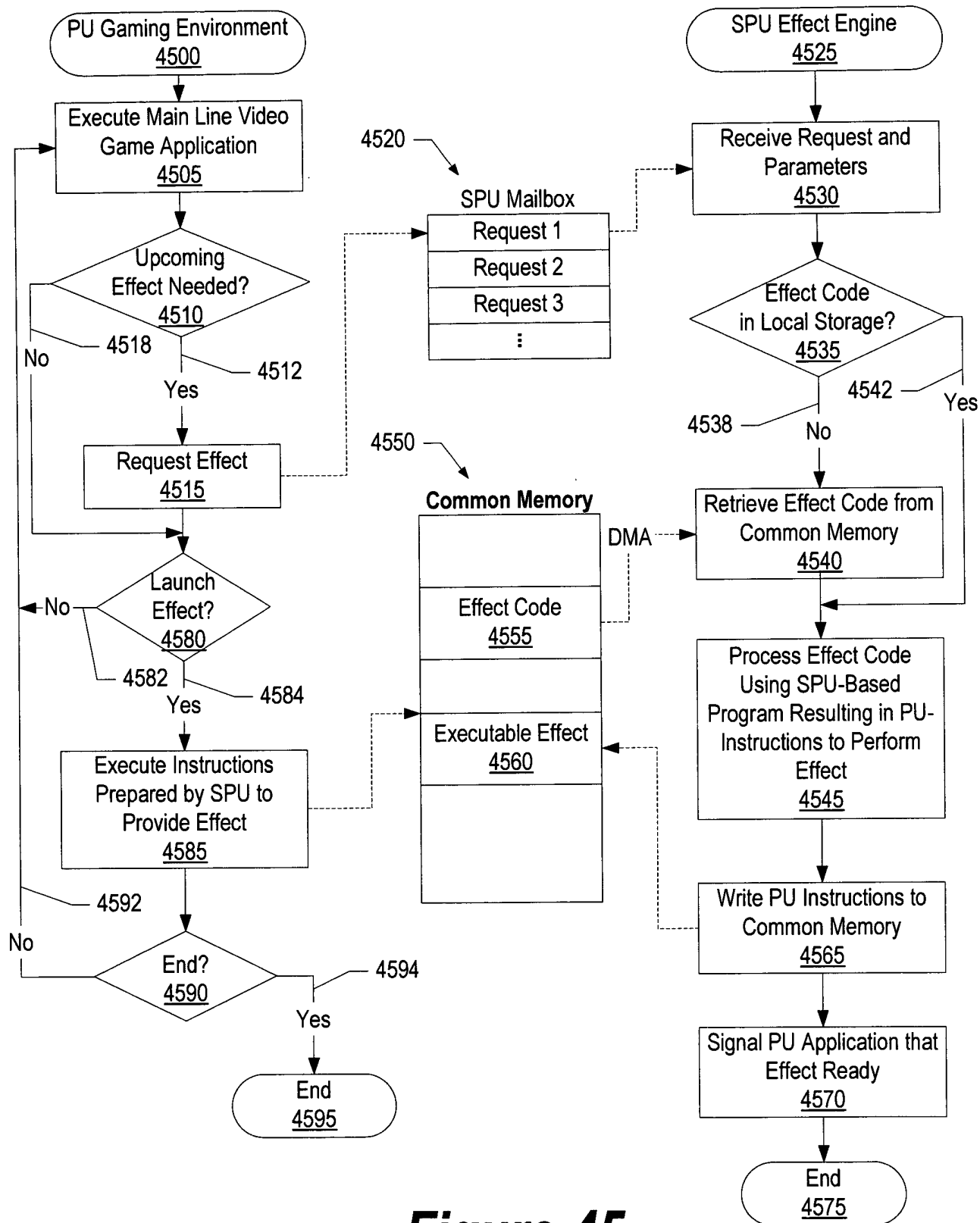
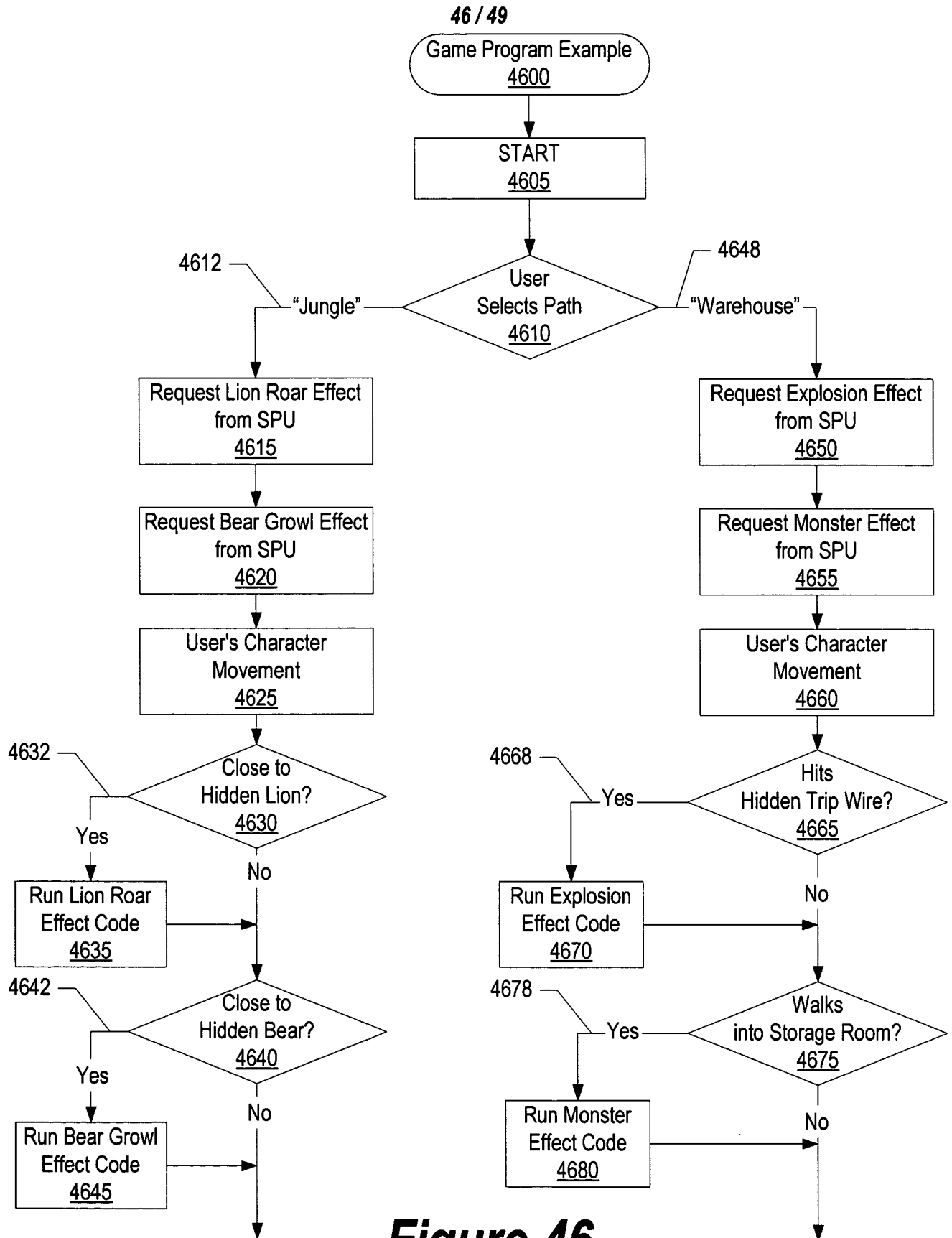


Figure 44

**Figure 45**

**Figure 46**

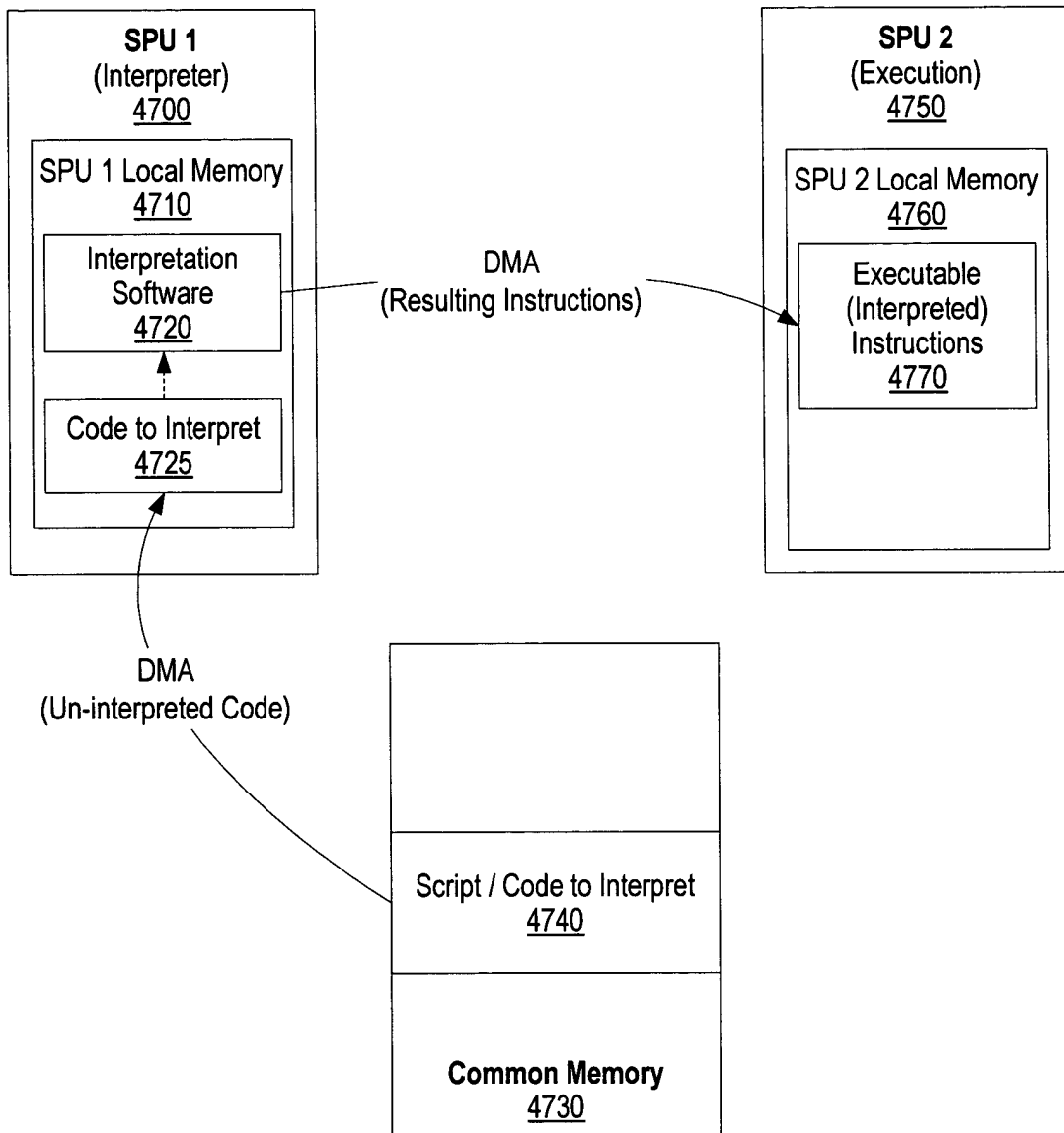


Figure 47

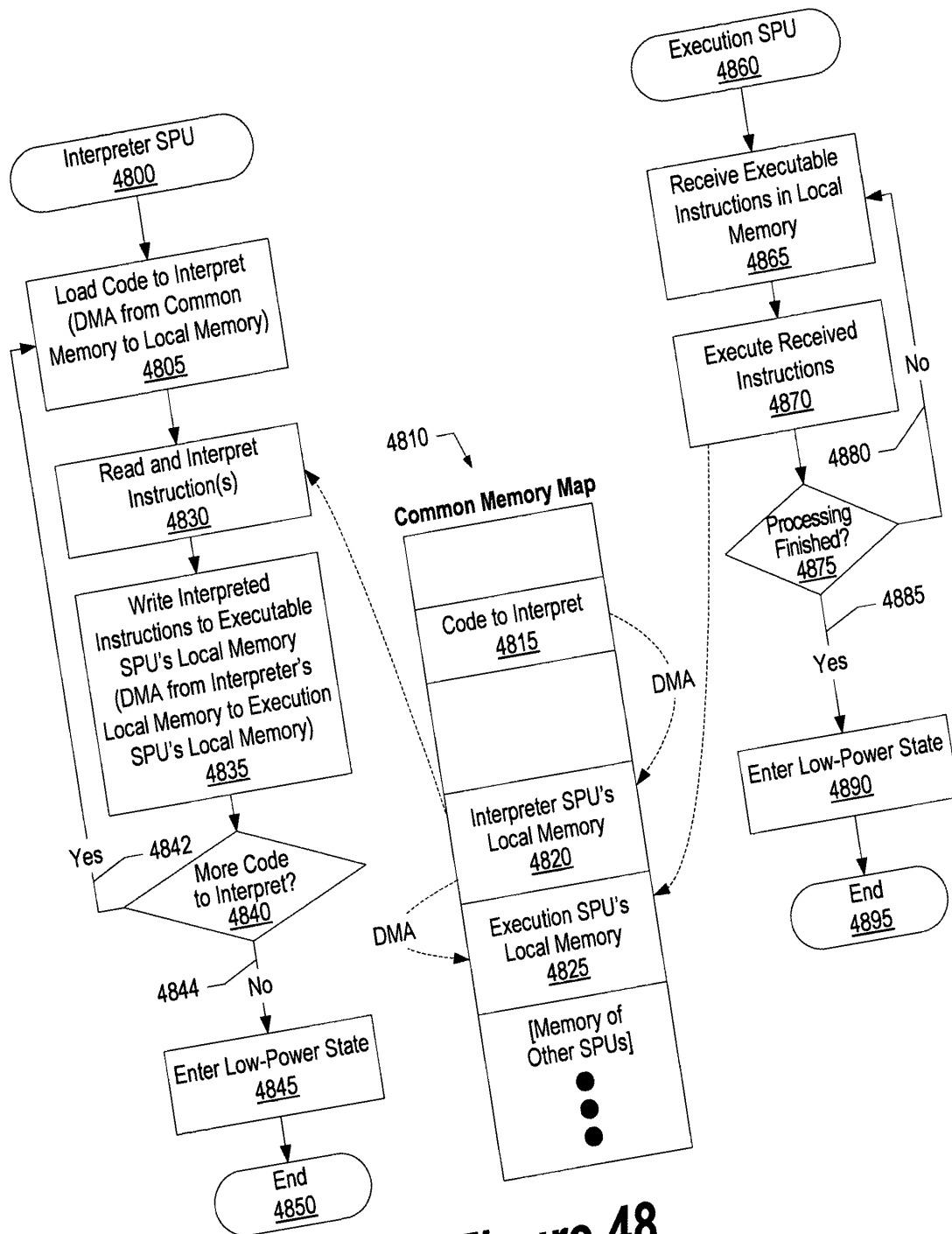
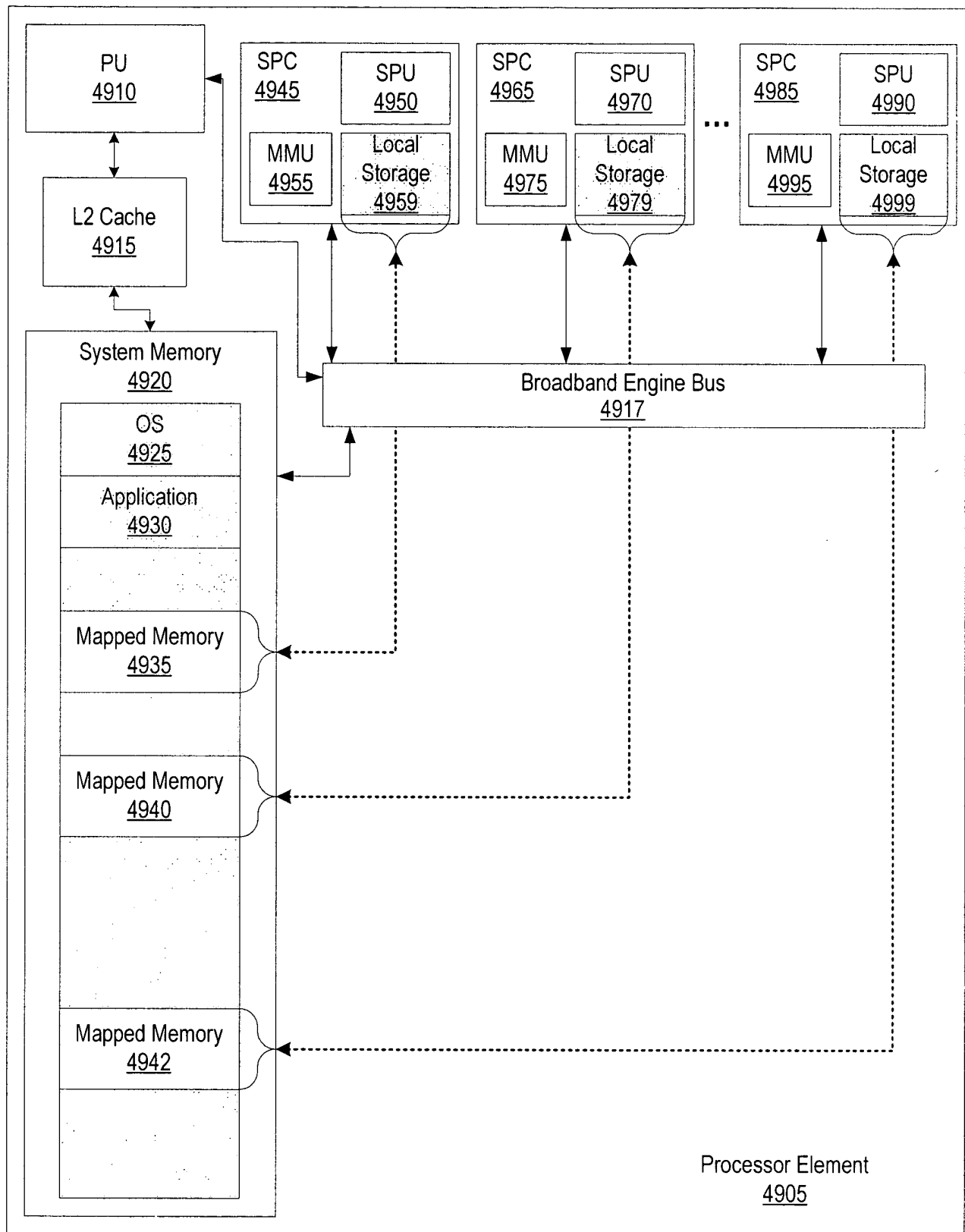


Figure 48

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**Figure 49**